

# Essentials Oak 14 Schematic

## Haswell-ULT

2013-4-19  
REV : X02

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*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DISCRTE OPTIMUS installed*

<Core Design>



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Title

**Cover Page**

Size

A3

Document Number

**OAK14 Haswell**

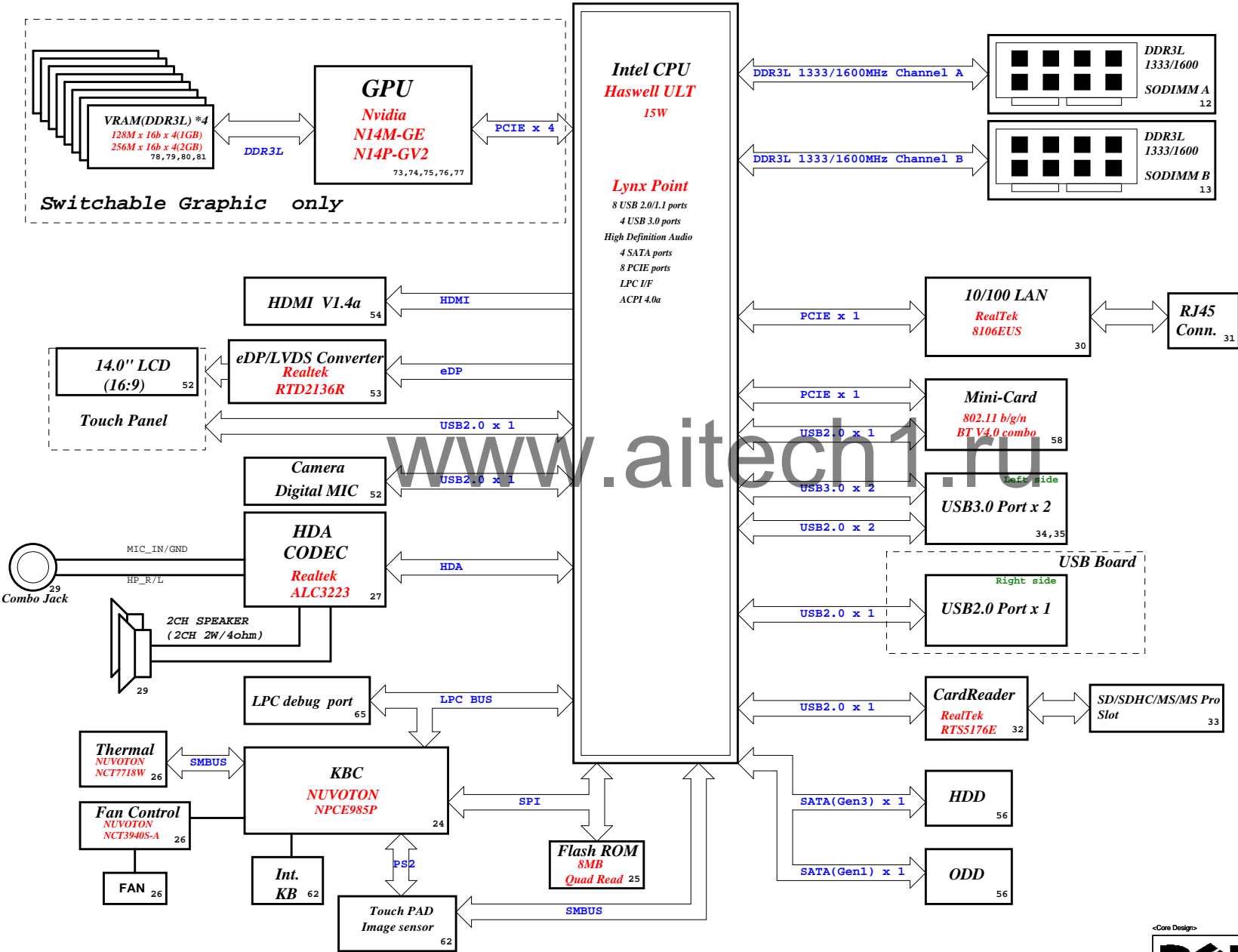
Rev

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Oak14 Block Diagram




CHARGER		
BQ24717		44
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
TPS51225		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core Power		46,47
ISL95813		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DDR3L SUS		49
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D65V_S0	
CPU 1.05V		48
RT8237		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
CPU 1D5V_S0		51
TLV70215		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
Switches		36 83
INPUTS	OUTPUTS	
1D35V_S3	1D35V_S0	
5V_S5	5V_S0	
3D3V_S5	0D675V_S0	
VCCP_CPU	3D3V_S0	
3D3V_S0	1D05V_VGA_S0	
	3D3V_VGA_S0	
	1D35V_VGA_S0	
PCB LAYER		
L1:Top	L5:VCC	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

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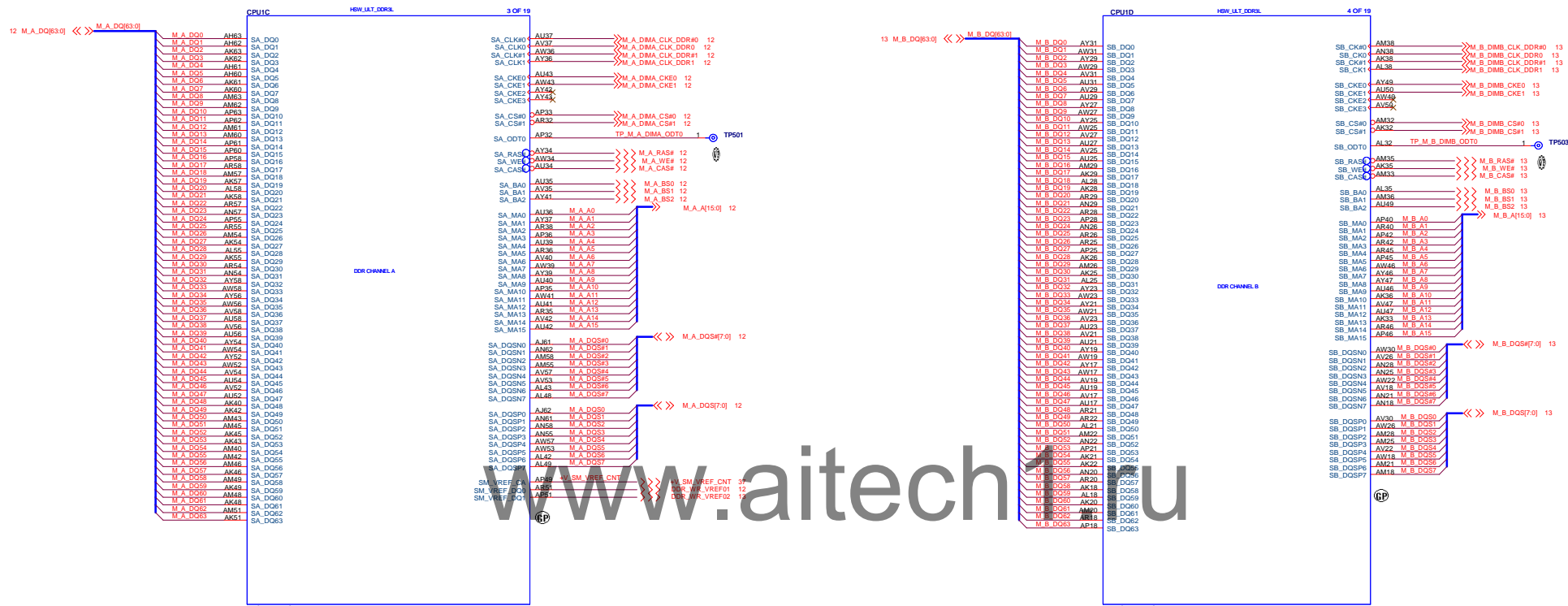
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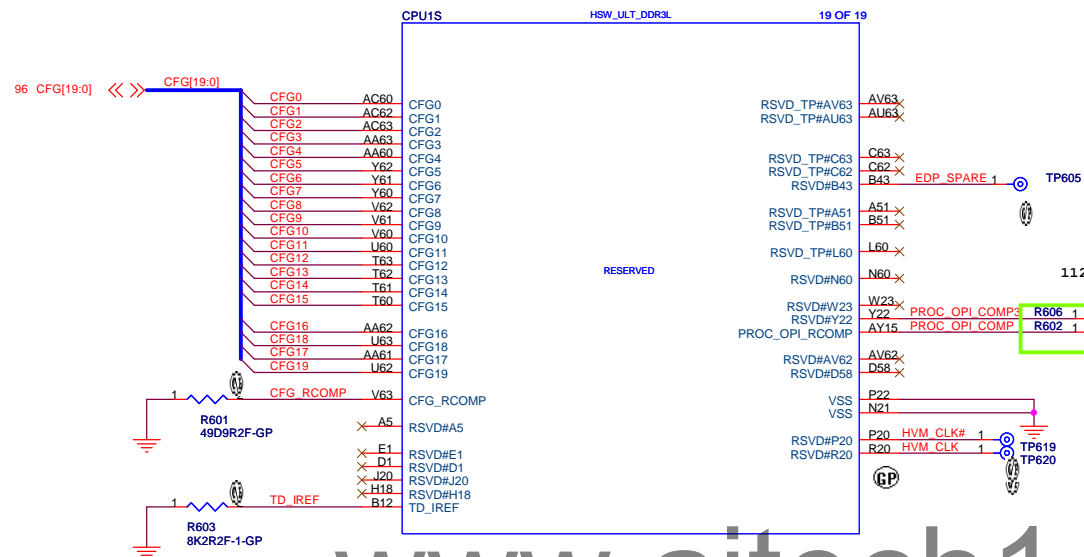


SSID = CPU



Title		
<b>CPU (DDR)</b>		
Size	Document Number	Rev
A2	<b>OAK14 Haswell</b>	<b>X00</b>
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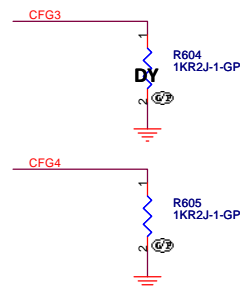
**SSID = CPU**



**Layout Note:**

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

## <Core Design>



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**CPU (RESERVED)**

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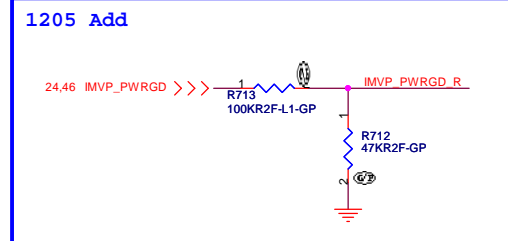
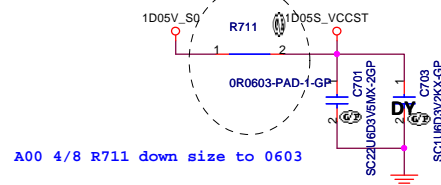
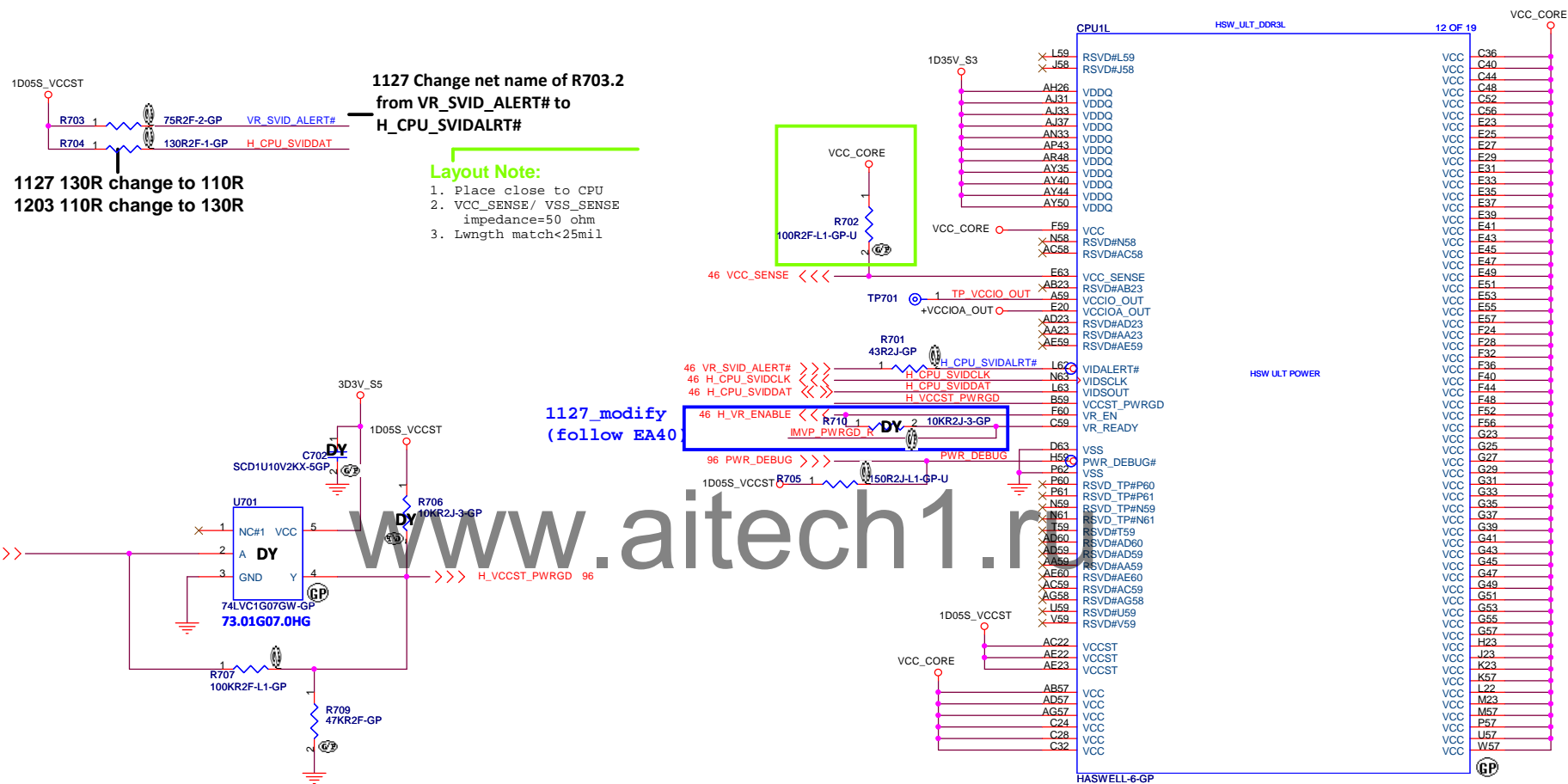
**OAK14 Haswell**

Rev	X00
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Date: Thursday, March 07, 2013

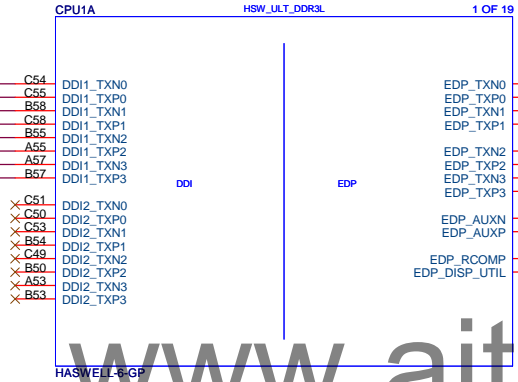
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**SSID = CPU**



HDMI

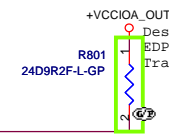
54 HDMI\_DATA2#  
54 HDMI\_DATA2  
54 HDMI\_DATA1#  
54 HDMI\_DATA1  
54 HDMI\_DATA0#  
54 HDMI\_DATA0  
54 HDMI\_CLK#  
54 HDMI\_CLK



EDP\_TXN0  
EDP\_TXP0  
EDP\_TXN1  
EDP\_TXP1  
EDP\_TXN2  
EDP\_TXP2  
EDP\_TXN3  
EDP\_TXP3  
EDP\_AUXN  
EDP\_AUXP  
EDP\_RCOMP  
EDP\_DISP\_UTIL

C45  
B46  
A47  
B47  
C47  
C46  
A49  
B49  
A45  
B45  
D20  
A43

EDP\_TX0\_DN 53  
EDP\_TX0\_DP 53  
EDP\_TX1\_DN 53  
EDP\_TX1\_DP 53  
EDP\_AUX\_DN 53  
EDP\_AUX\_DP 53  
EDP\_COMP  
EDP\_BRIGHTNESS



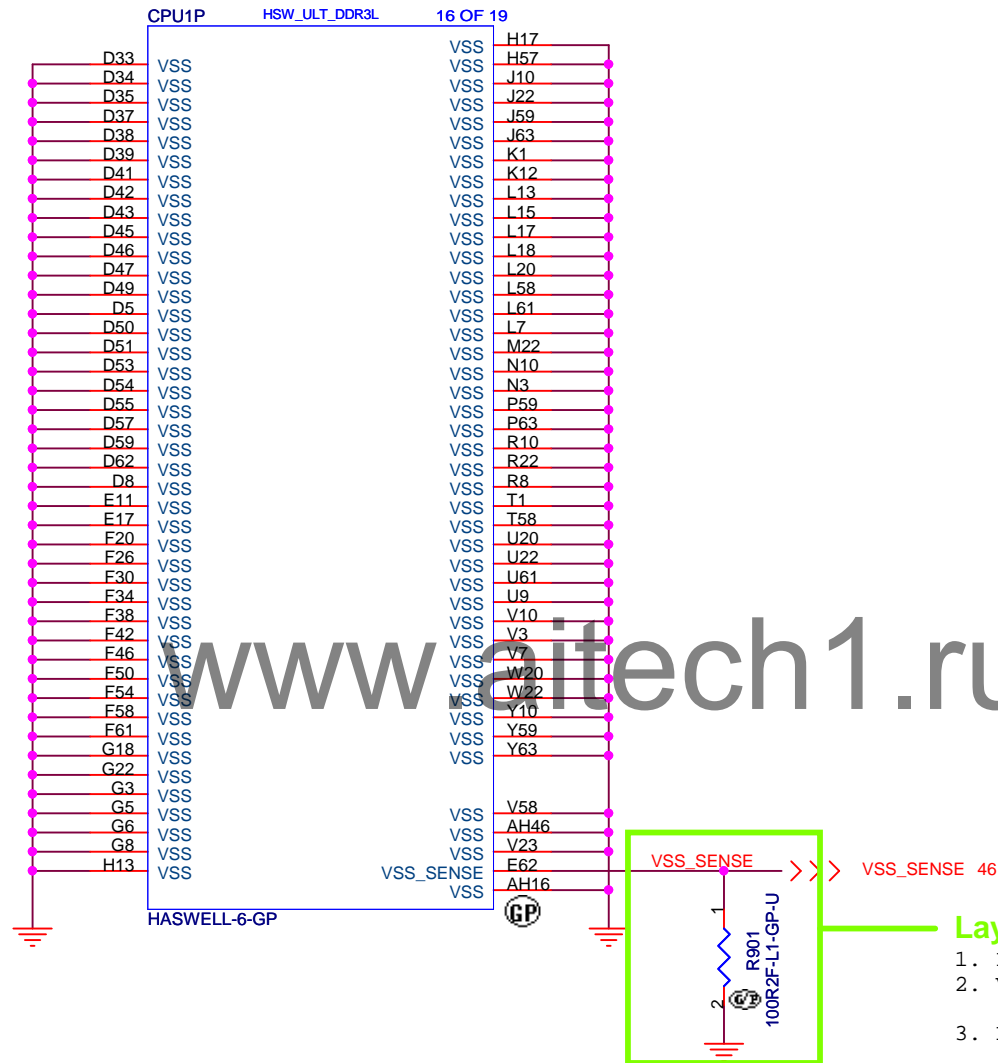
Design Guideline:  
EDP\_COMP keep routing length max 100 mils.  
Trace Width:20 mils.

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Title <b>CPU (DDI/EDP)</b>			
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SSID = CPU



**Layout Note:**

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Lwngth match<25mil

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Title

**CPU (VSS)**

Size  
A4

Document Number

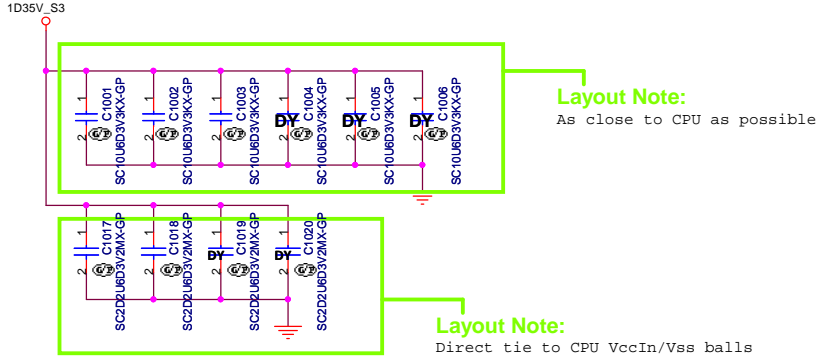
**OAK14 Haswell**

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**X00**

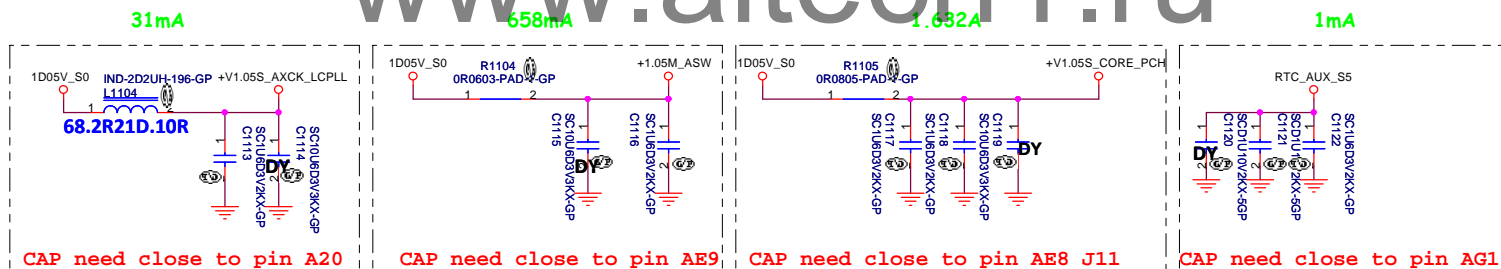
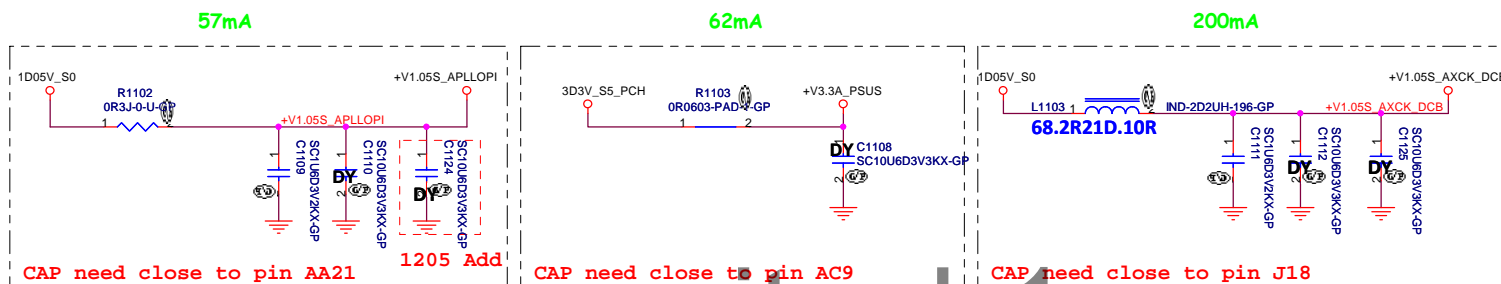
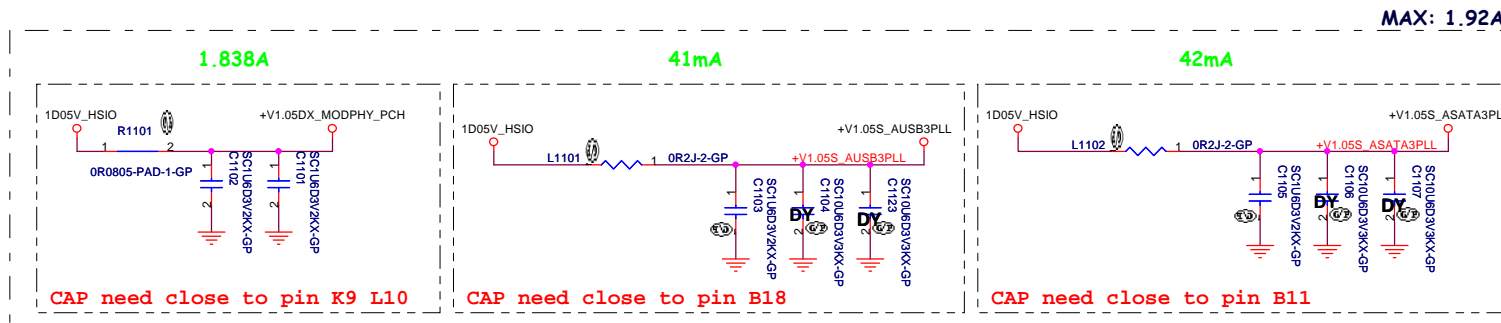
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SSID = CPU



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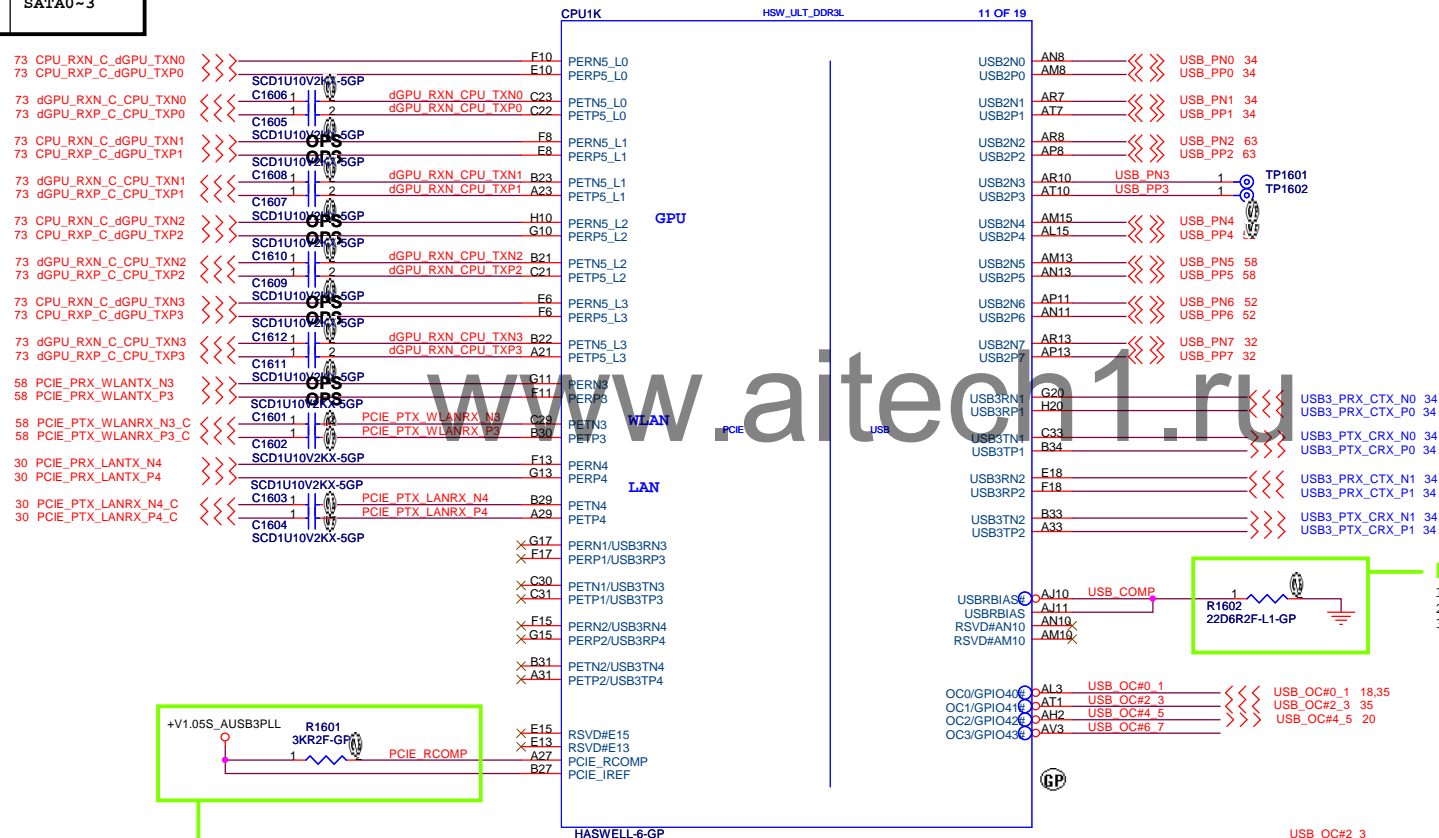
SSID = PCH

## PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	LAN	
5(4lane)	GPU	
6(4lane)	TBD	SATA0~3

## USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3
3	TBD
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader



### Layout Note:

1. PCIE\_RCOMP/ PCIE\_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

### Layout Note:

1. USB\_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

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Title

**PCH (PCIE/USB)**

Size

Document Number

**OAK14 Haswell**

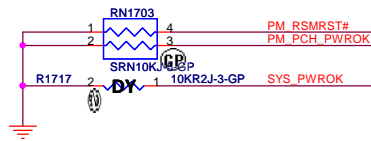
Rev

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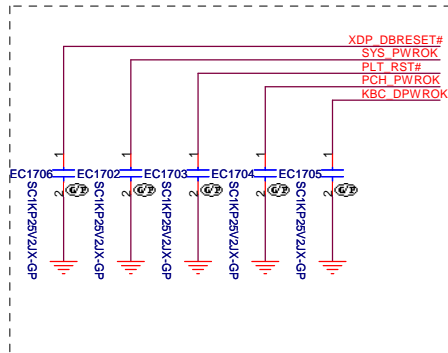
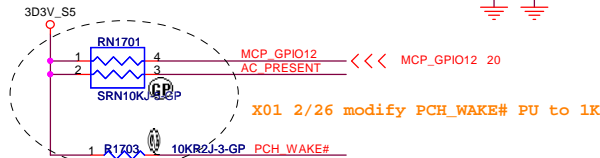
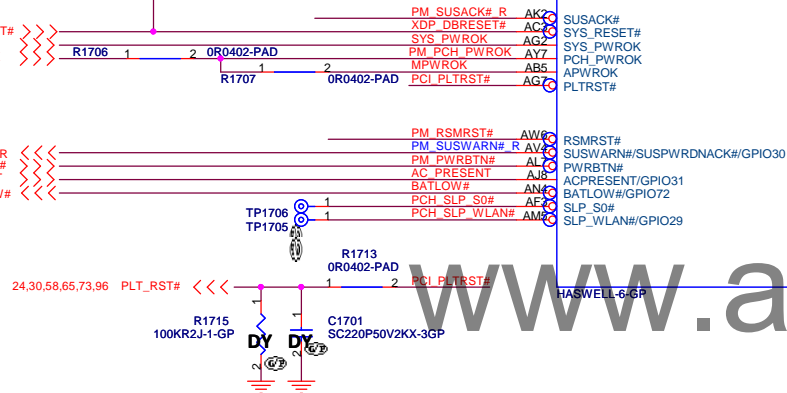
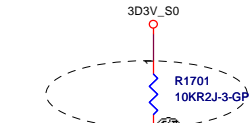
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**SSID = PCH**



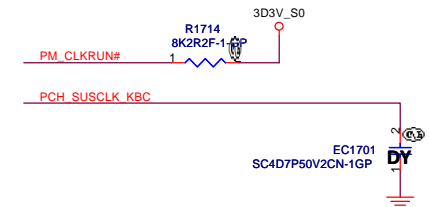
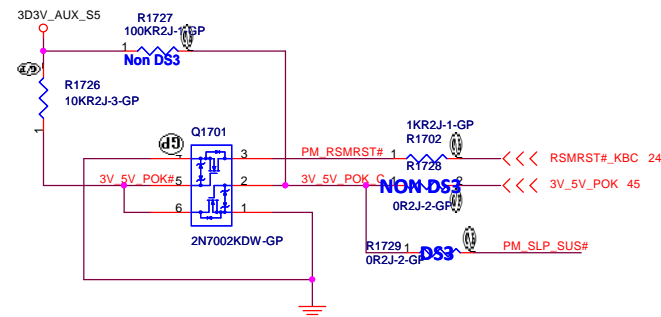
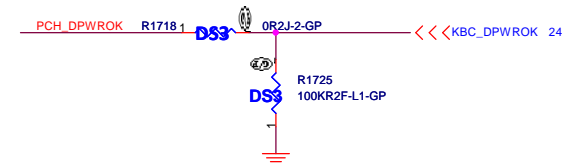
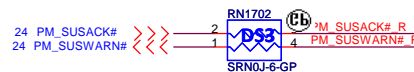
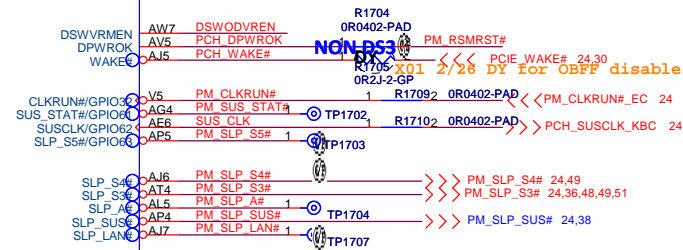
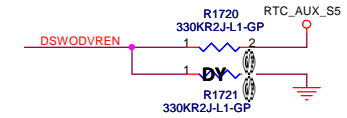
X01 2/26 Add PH 10K on XDP\_DBRESET#



EMI 12/20

**PCH strap pin:**

On Die DSW VR Enable	
DSWODVREN	Low = Disable * High = Enable (default)



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**PCH (PM)**

Size  
A3

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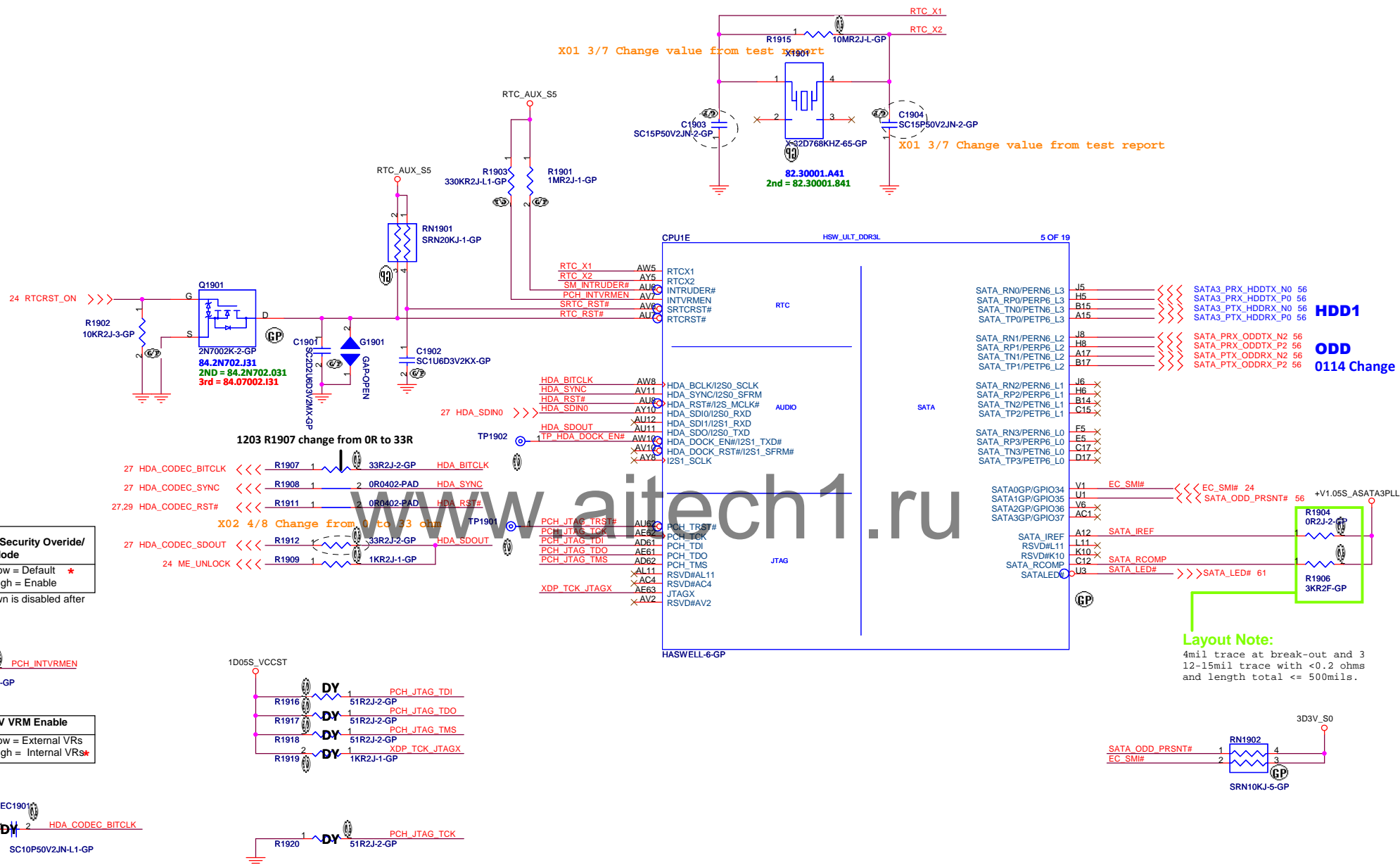
**OAK14 Haswell**Rev  
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SSID = CPU



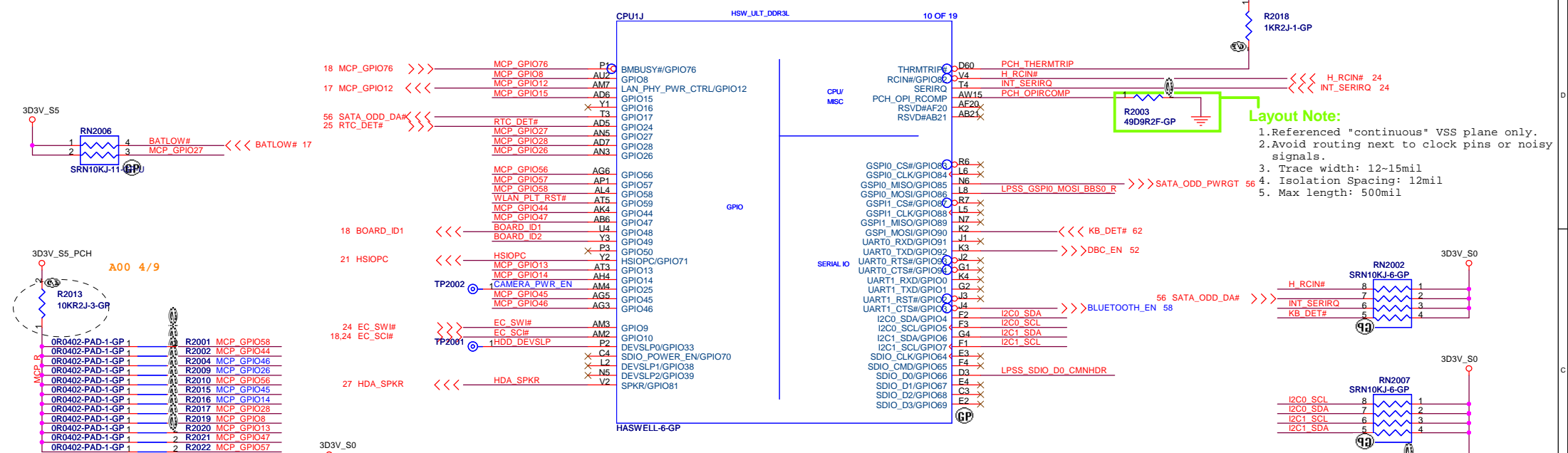
**Layout Note:**  
4mil trace at break-out and 3  
12-15mil trace with <0.2 ohms  
and length total <= 500mils.

<b>Flash Descriptor Security Override/ Intel ME Debug Mode</b>	
<b>HDA_SDOUT</b>	Low = Default <span style="color: red;">★</span> High = Enable

The internal pull-down is disabled after PLTRST# deasserts

<b>Integrated SUS 1V VRM Enable</b>	
<b>INTVRMEN</b>	Low = External VRs High = Internal VRs*

SSID = CPU



**PCH strap pin:**

18,30	NO REBOOT
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

**Top-Block Swap Override mode**

SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) * Low = Disable "Top-Block swap" mode
------------------	--

The internal pull-down is disabled after PLTRST# deasserts

**TLS Confidentiality**

GPIO15	* Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS
--------	--

The internal pull-down is disabled after RSMRST# deasserts.

**Boot BIOS Strap Bit BBS**

Boot BIOS Destination	* Low = SPI High = LPC
-----------------------	---------------------------

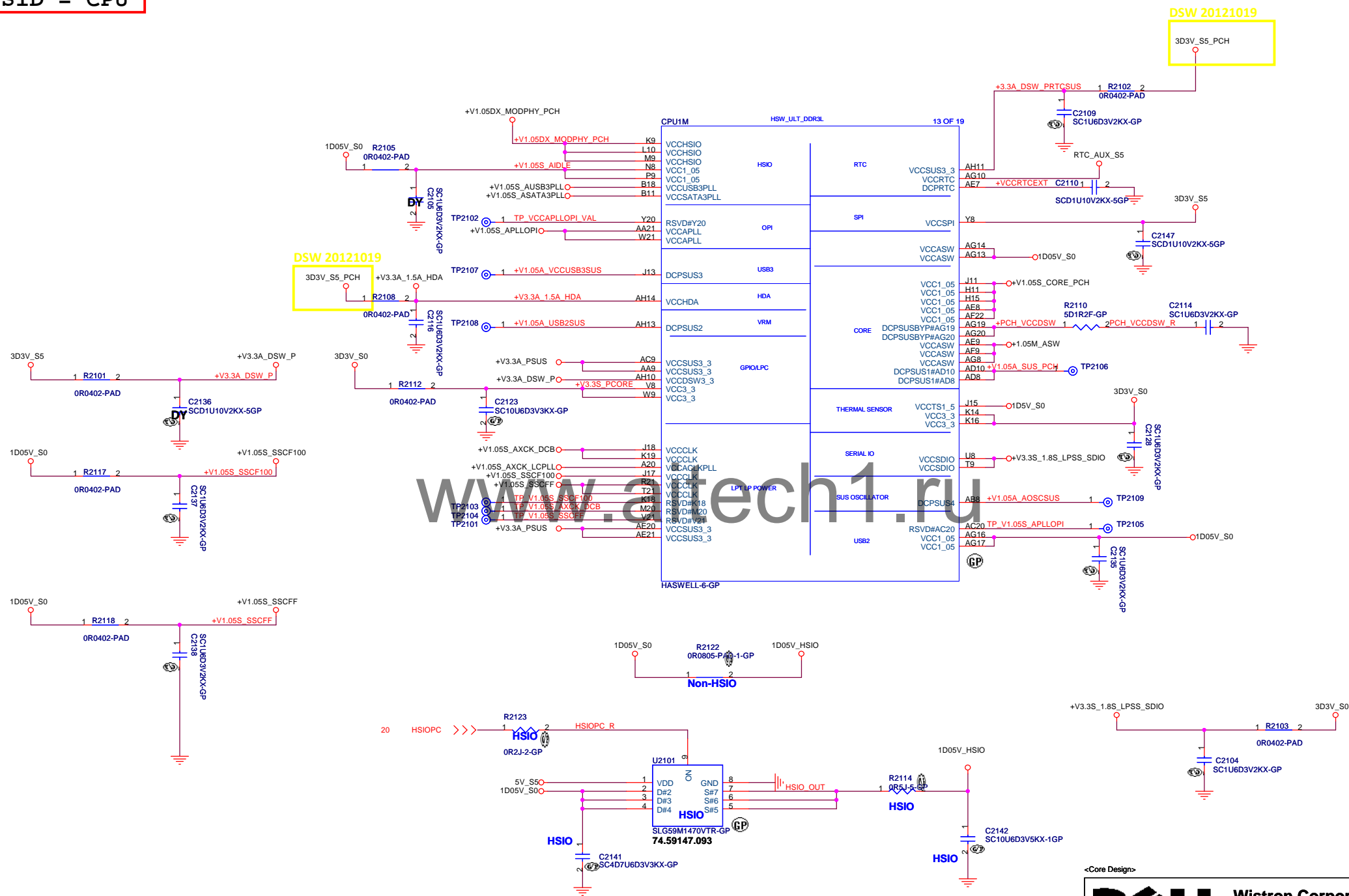
The internal pull-down is disabled after PLTRST# deasserts

**BIOS strap pin:**

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
UMA	1	0
DIS	1	1



**SSID = CPU**



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**CPU (POWER2)**Size  
A

Document Number

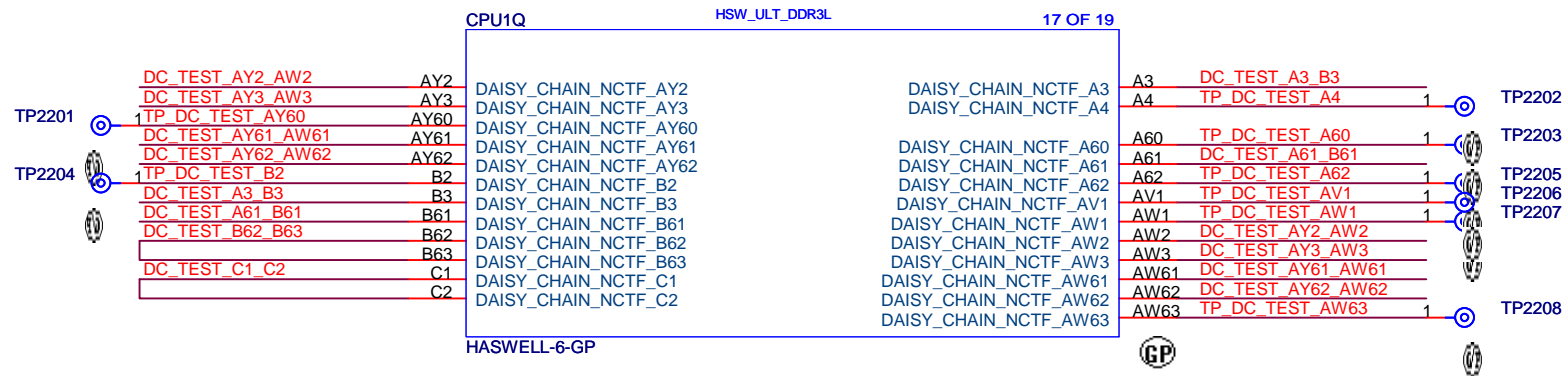
**OAK14 Haswell**

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SSID = PCH



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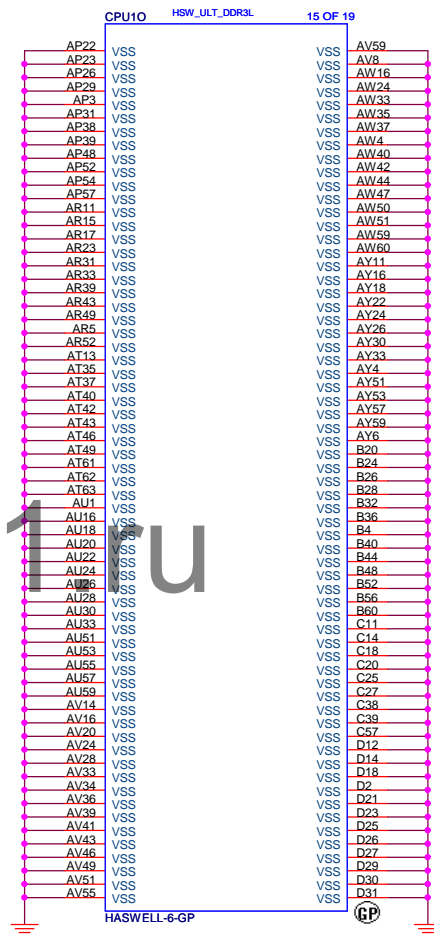
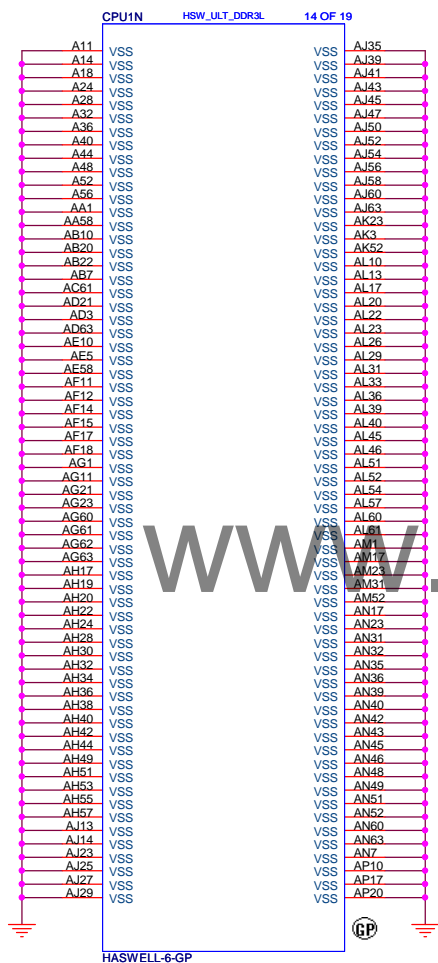
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SSID = PCH



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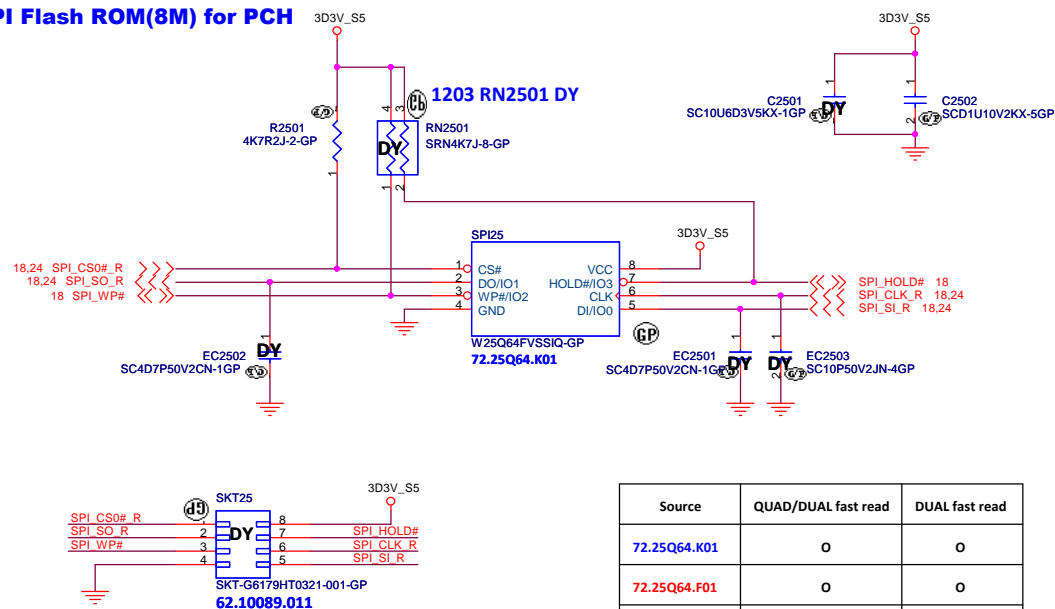
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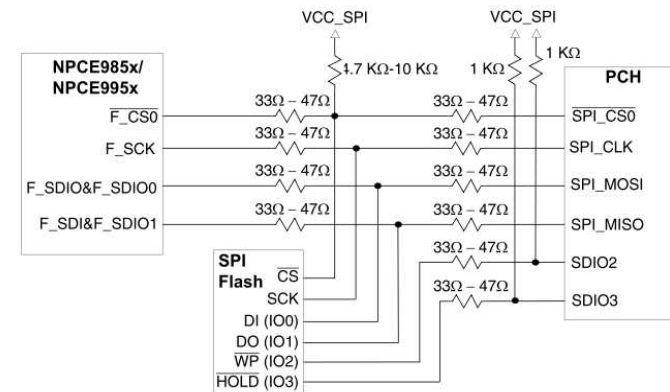
**SSID = Flash.ROM**

### SPI Flash ROM(8M) for PCH



Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	0	0
72.25Q64.F01	0	0
72.25Q64.D01	0	0

### Single SPI shared flash connection (SPI Quad I/O mode)

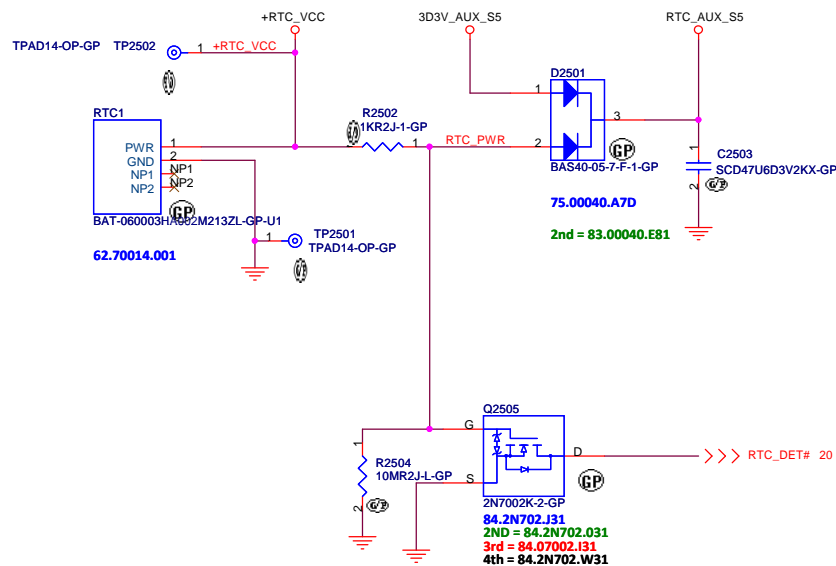


Refer to "NCPE985x/ NPCE995x board design reference guide"

72.25Q64.D01	0	0
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**SSID = RBATT**



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## Flash/RTC

Size  
A3

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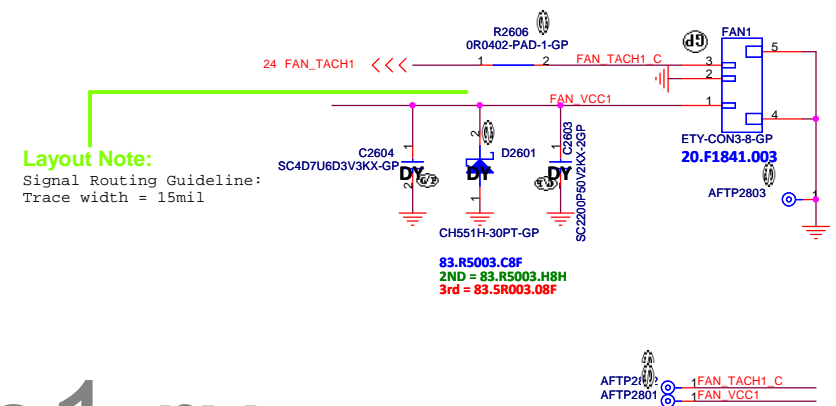
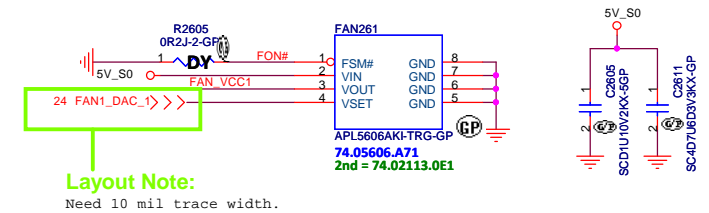
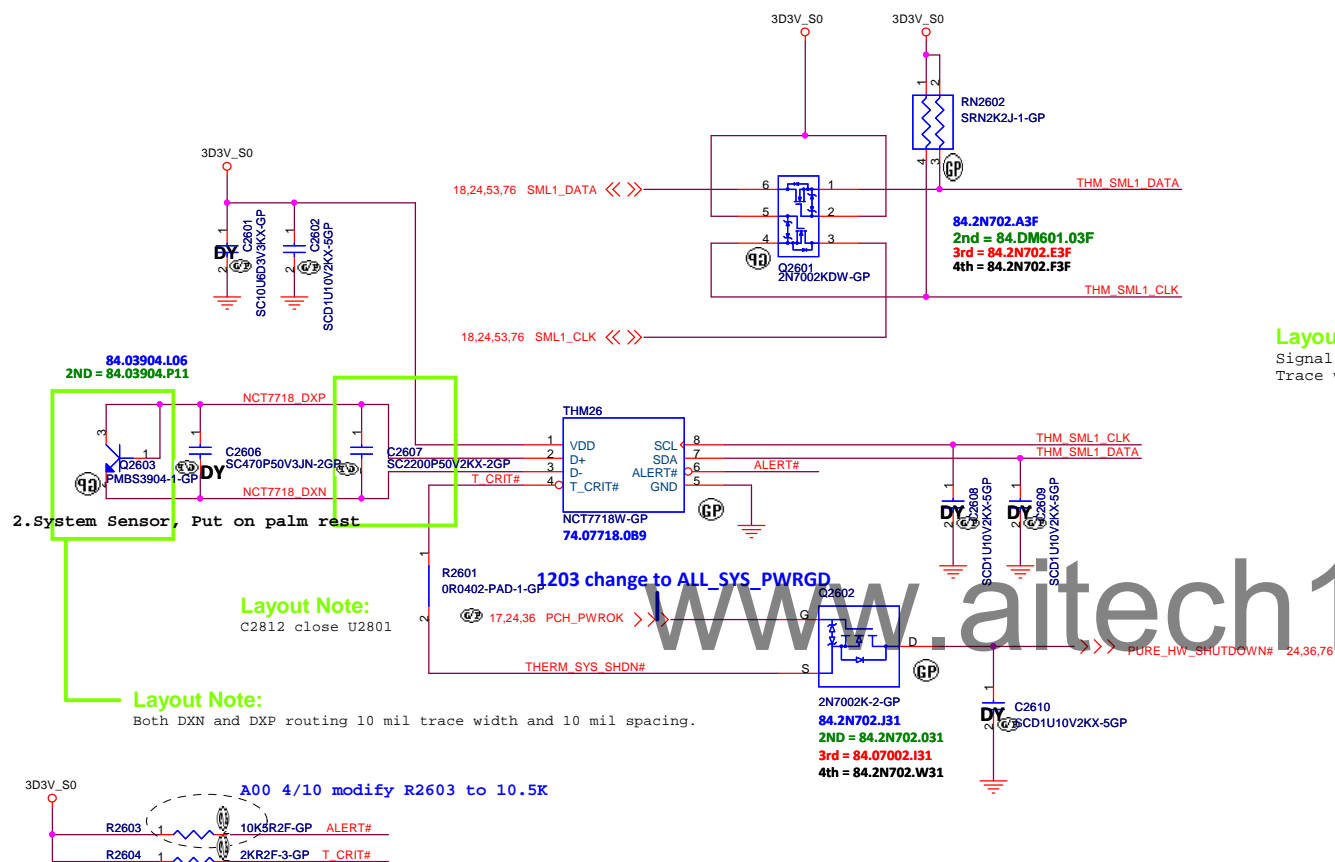
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SSID = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



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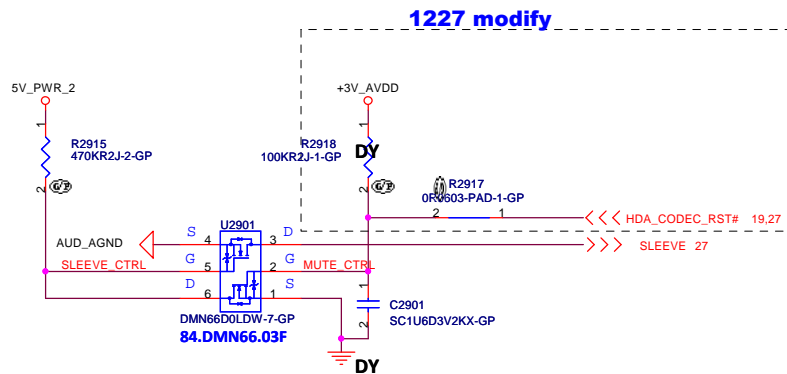
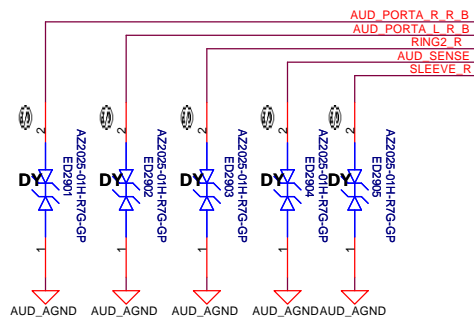
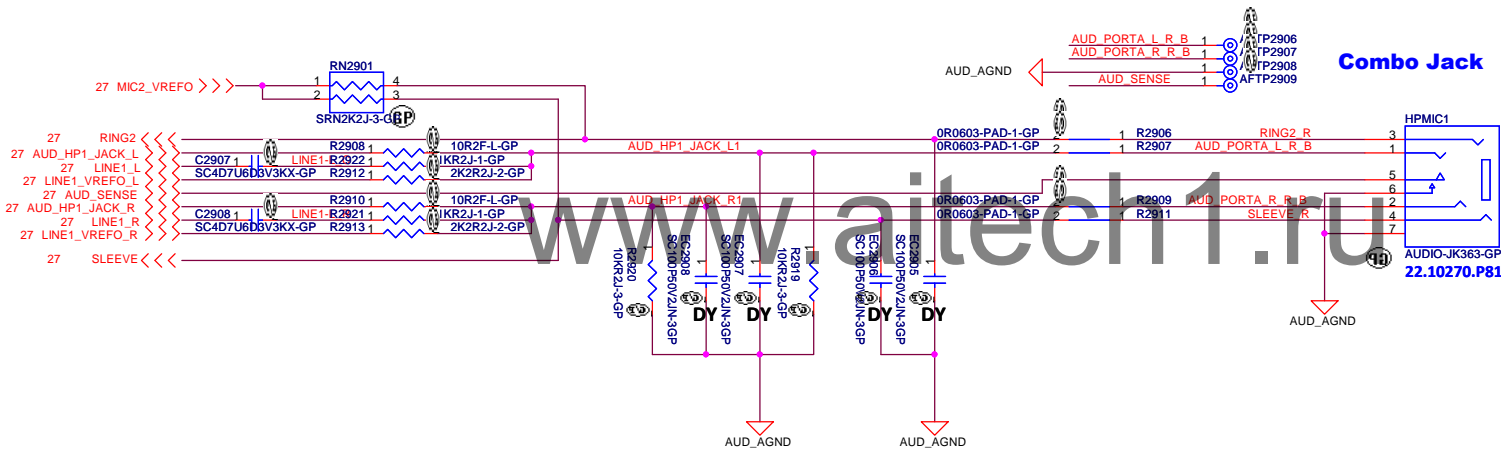
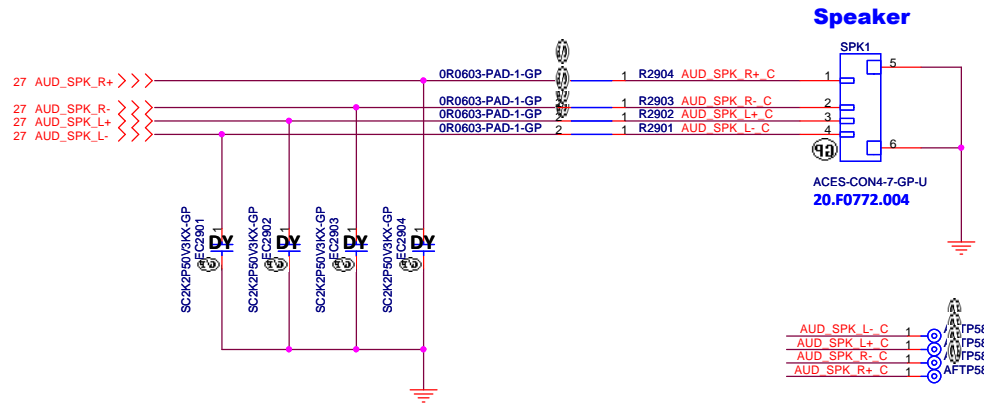
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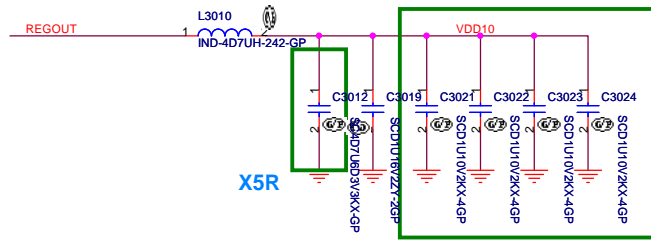


SSID = AUDIO

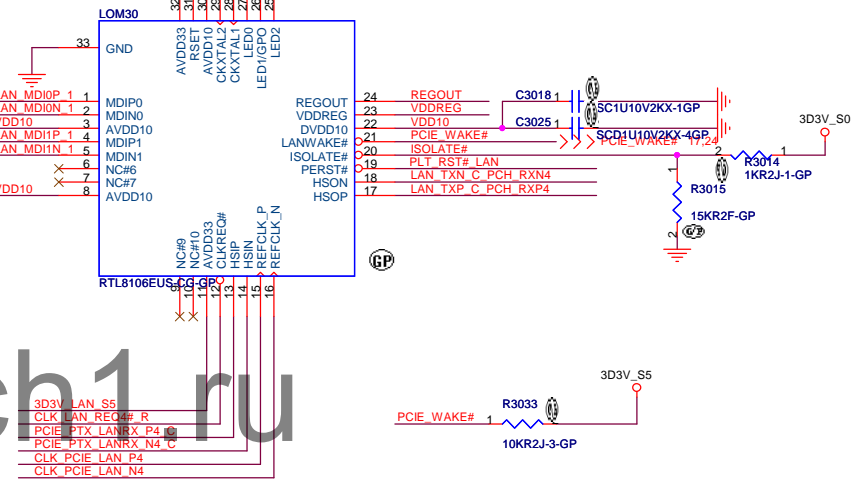
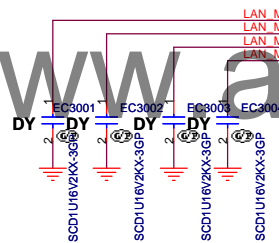
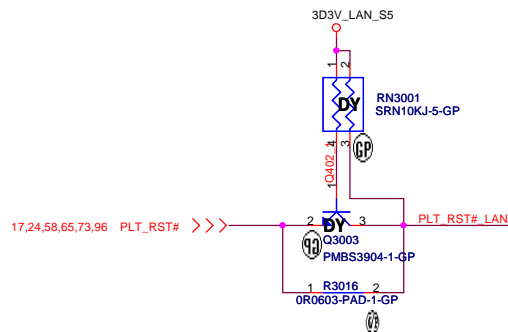
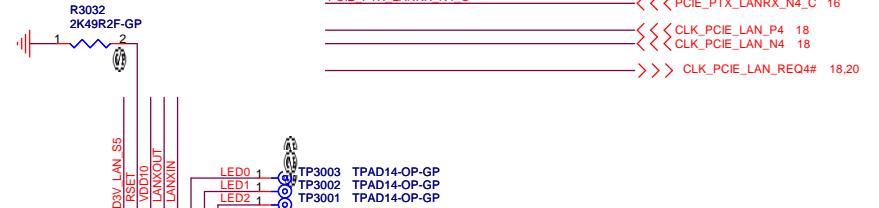
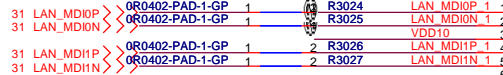
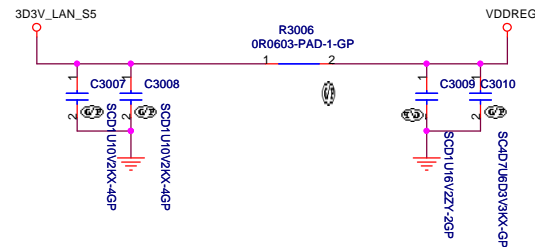


## LAN CHIP

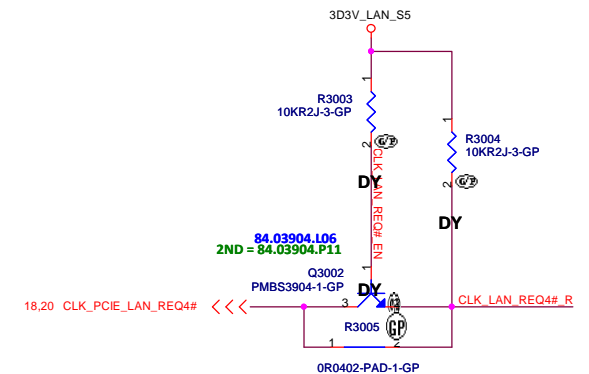
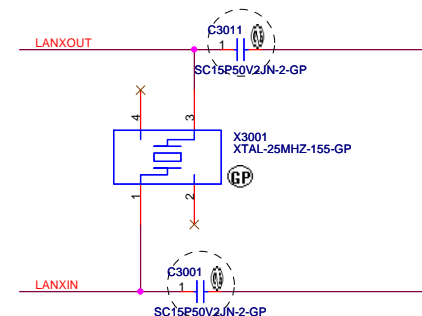
10/100 Need Only need C3021, C3022, C3023, C3024 in Pin3, 8, 22, 30



40 mils



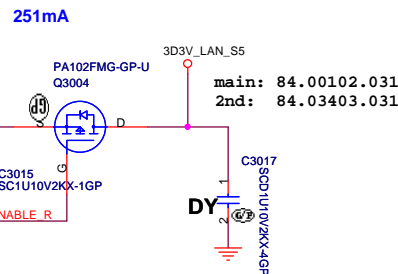
X01 3/7 Change value from test report



24 PM\_LAN\_ENABLE >>>

R3023  
100KR2J-1-GP

2N7002K-2-GP



## <Core Design>



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Title

**LOM**

Size  
A3

Document Number
-----------------

**OAK14 Haswell**

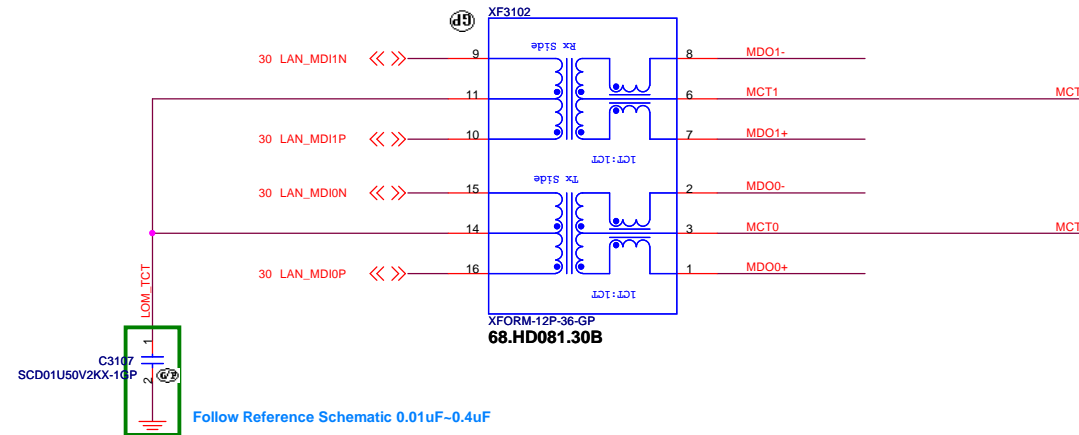
Rev	X00
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Date: Wednesday, April 17, 2013

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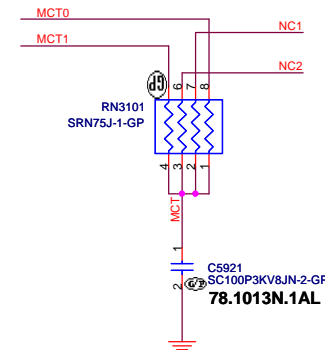
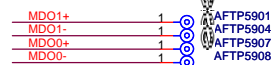
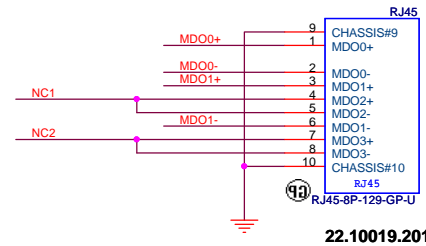
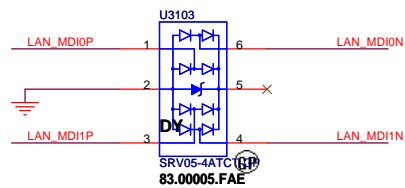
SSID = LOM

## 10/100 LAN TransFormer



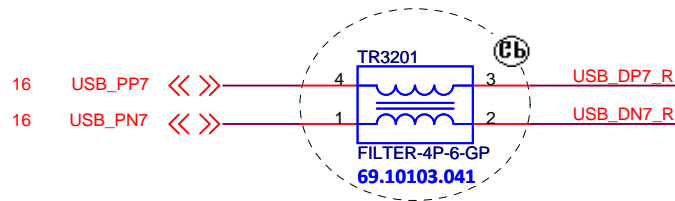
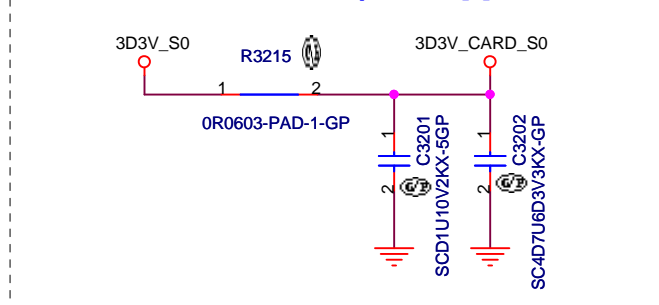
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## RJ45 CONN



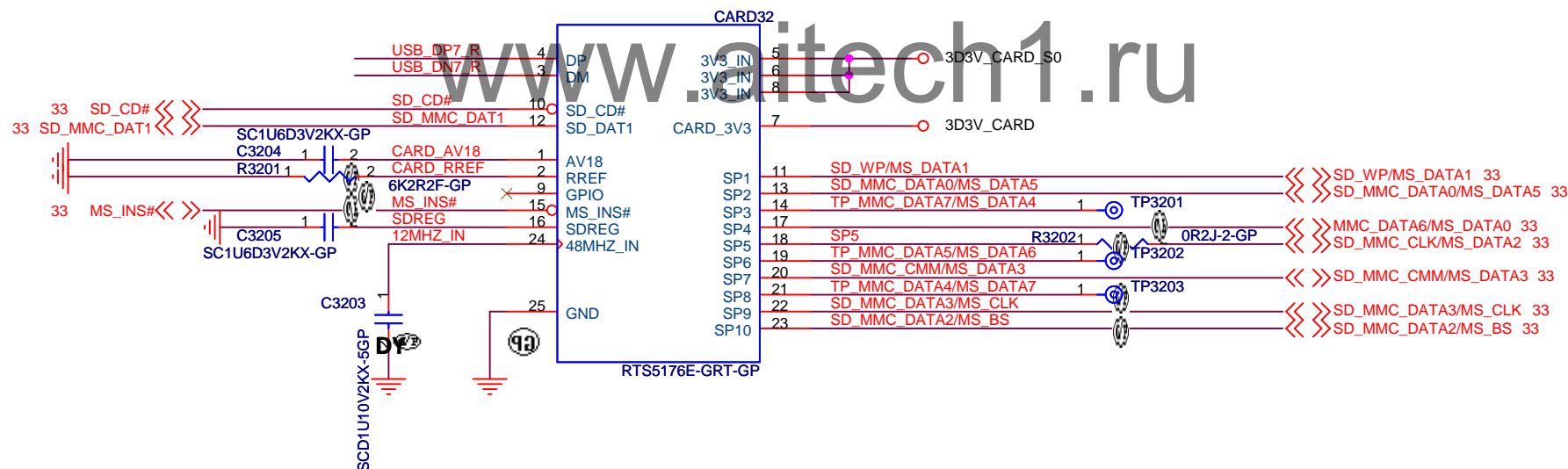
<Core Design>

## 1121 remove Switch(No support D3 cold)



A00 4/10 Add TR3201

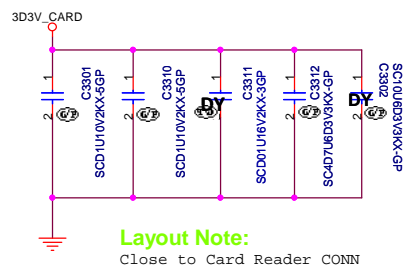
Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



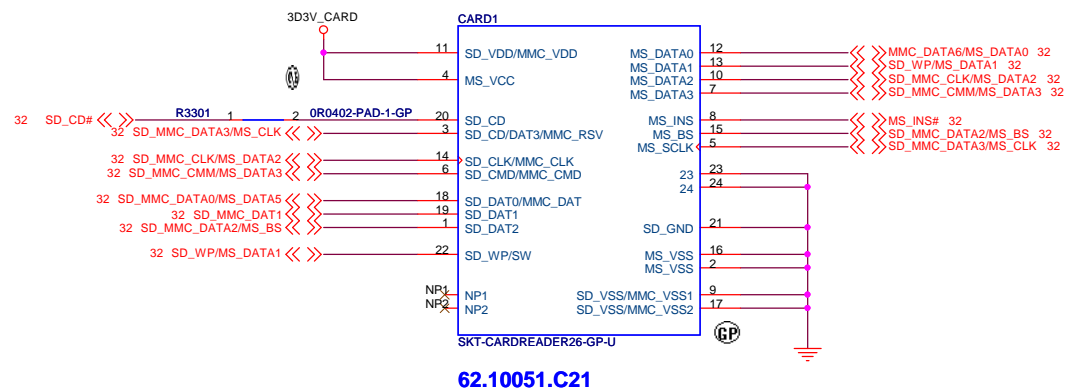
<Core Design>

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		<b>Card Reader-RTS5176</b> <b>OAK14 Haswell</b>	
Size A4	Document Number	Date: Wednesday, April 17, 2013	Rev X00
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SSID = SDIO

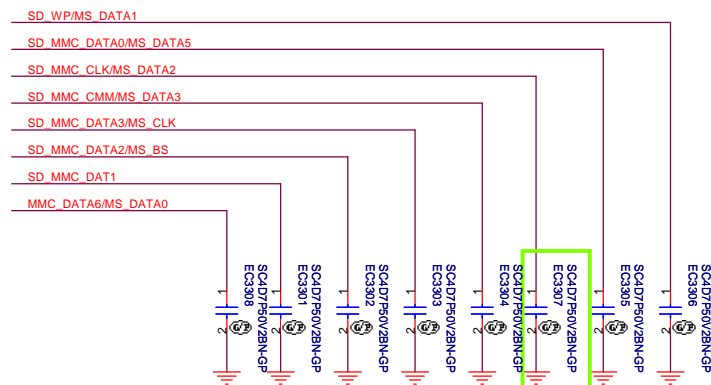


### SD/MS/MMC Card Connector



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### For EMI Reserved



Layout Note:  
please close U3201

1203 modify 10P change to 4.7P

<Core Design>



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SD/XD/MS/MMC Card CONN

Size

A3

Document Number

OAK14 Haswell

Date: Tuesday, April 16, 2013

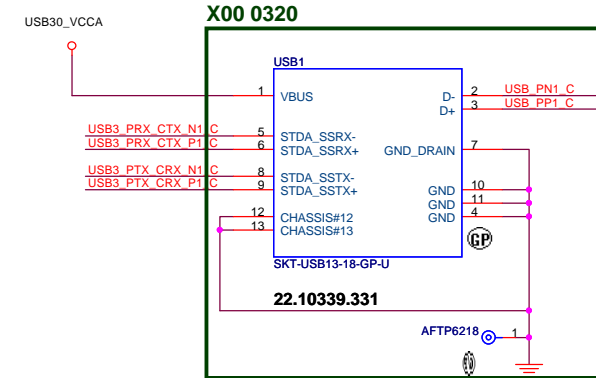
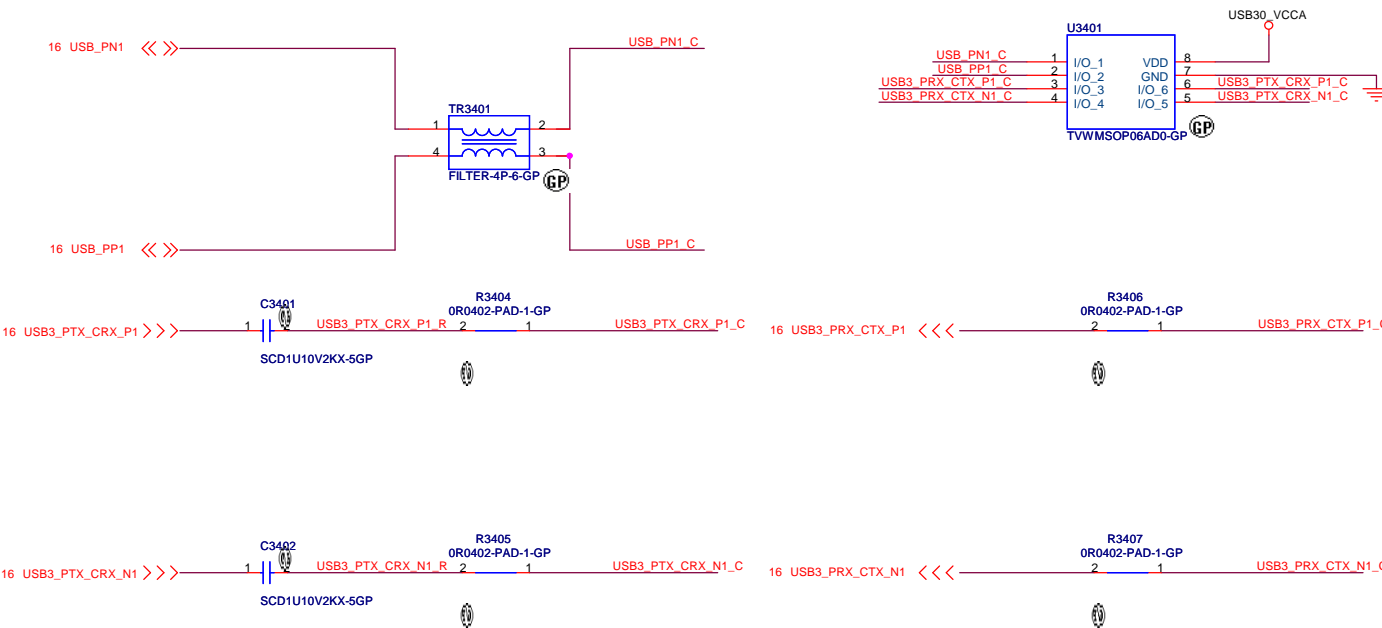
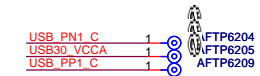
Sheet 33 of 104

Rev

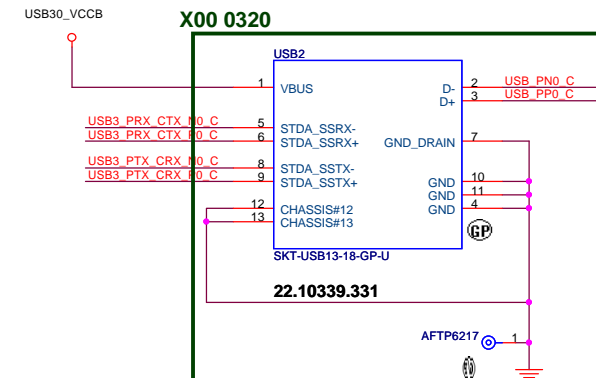
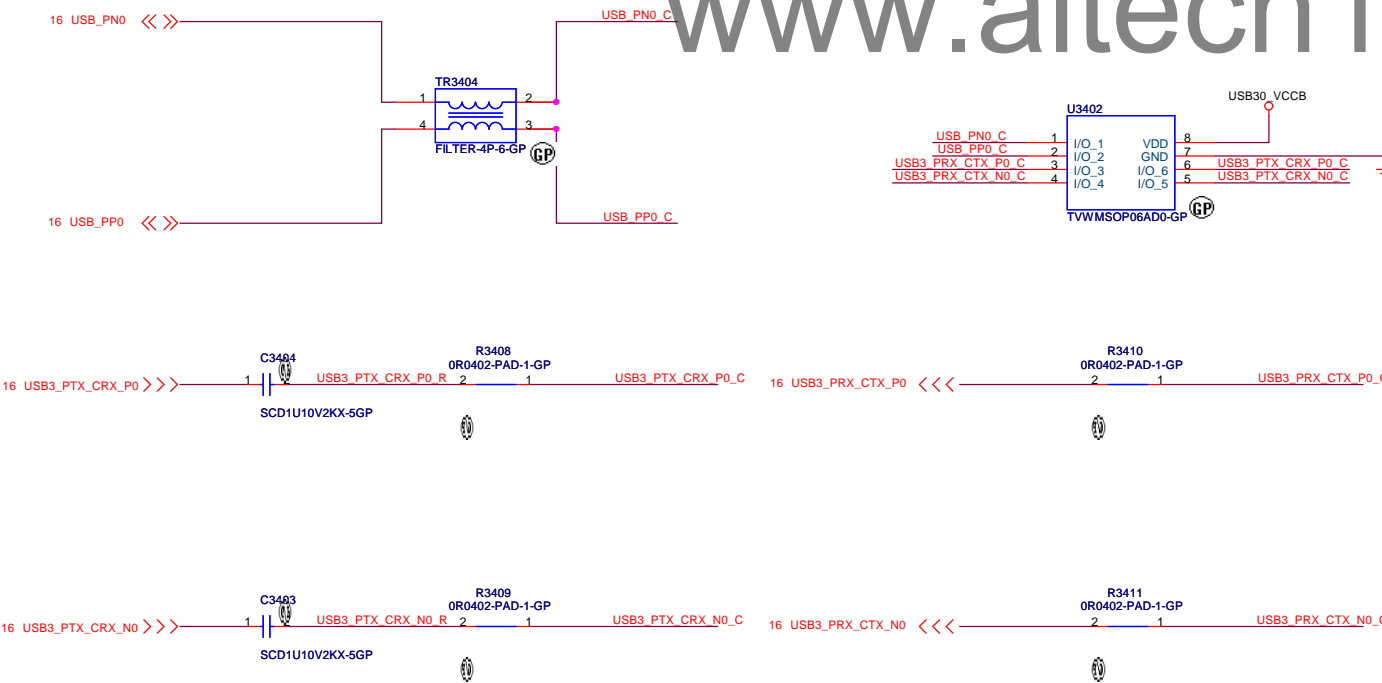
X00

SSID = USB

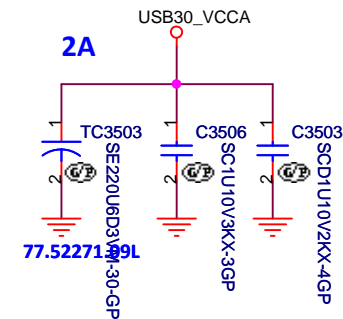
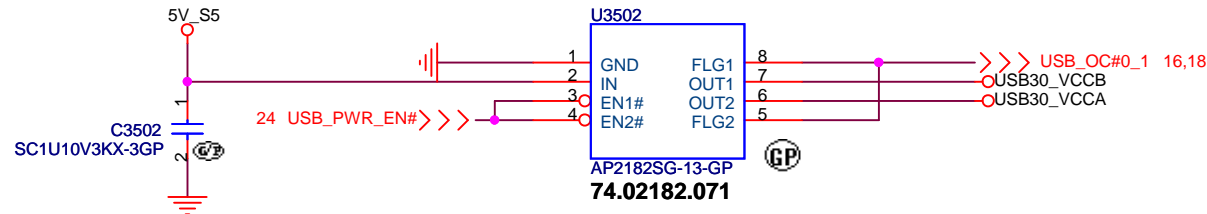
## USB3.0 Port1



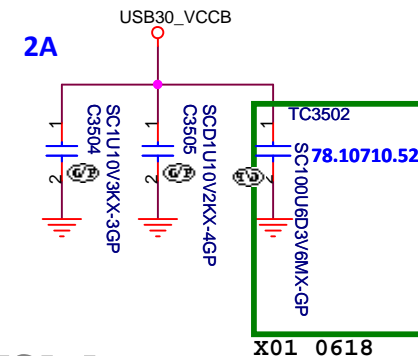
## USB3.0 Port2



<Core Design>



**USB3.0 Port1**

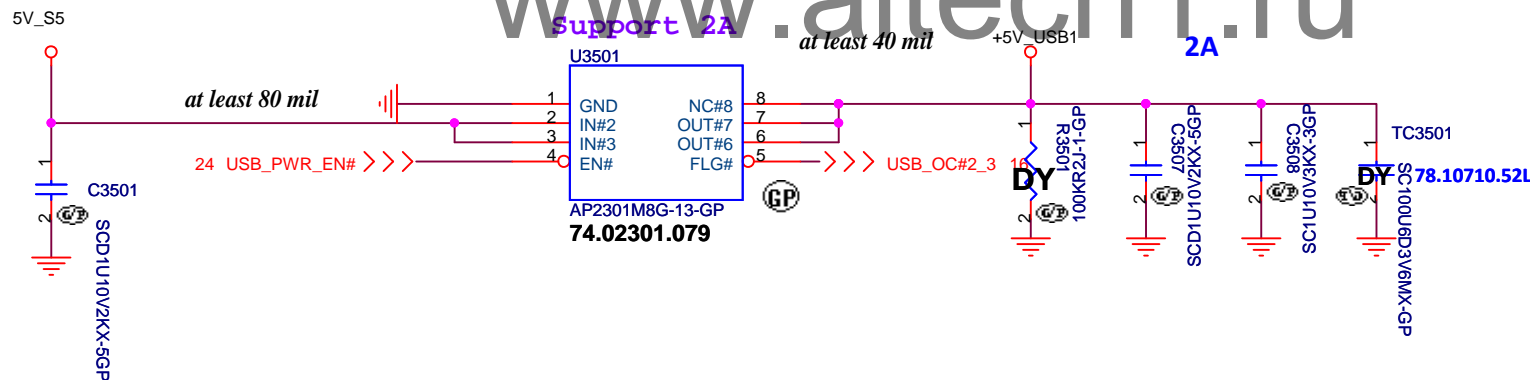


**USB3.0 Port2**

## Right USB Power x1

Support 2A

at least 40 mil



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Title

**USB Power SW**

Size

Document Number

**OAK14 Haswell**

Rev

**X00**

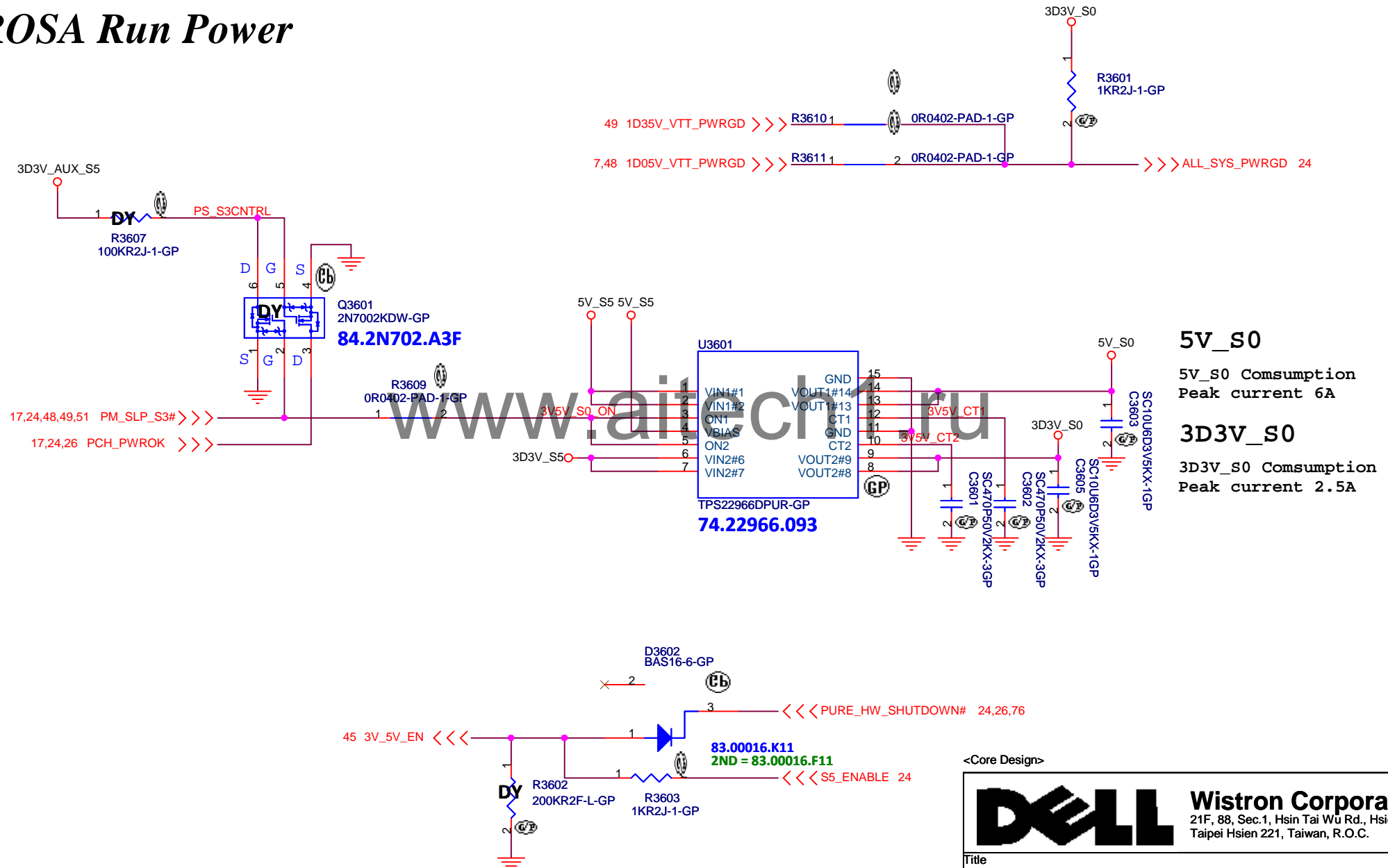
Date: Monday, April 15, 2013

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```
SSID = Reset.Suspend
```

# Power Good

## ***ROSA Run Power***



## <Core Design>



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Title

## Power Plane Enable

Size

Document Number

# OAK14 Haswe

V

X00

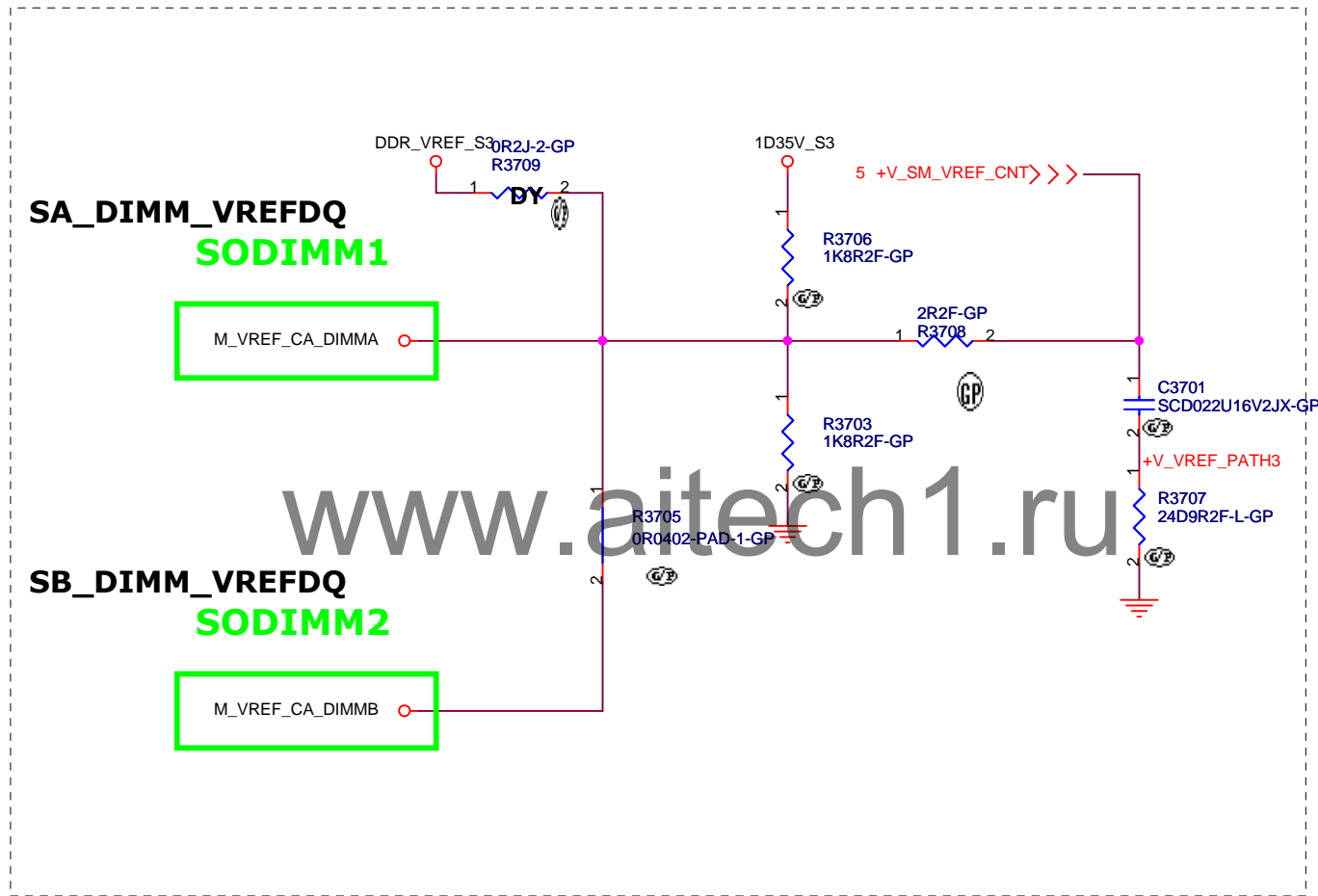
Date: Wednesday, April 17, 2013

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**Layout Note:**

Place Close SO-DIMM



<Core Design>



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Title

**S3 Reduction Circuit**

Size  
A4

Document Number

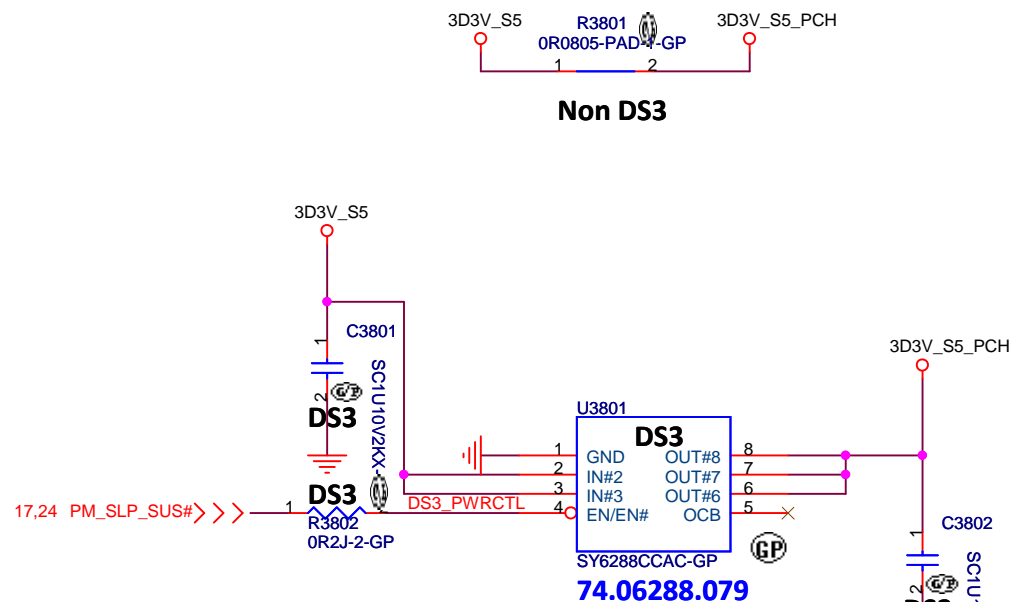
**OAK14 Haswell**

Rev

**X00**

Date: Wednesday, April 17, 2013

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1210 change power switch (RdsON:100m ohm)

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>DSW</b>			
Size A4	Document Number <b>OAK14 Haswell</b>		Rev <b>X00</b>
Date: Wednesday, April 17, 2013	Sheet 38	of	104

SSID = CPU

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<Core Design>



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Title		<b>CPU (POWER1)</b>	
Size	Document Number	Rev	
Custom	<b>OAK14 Haswell</b>	<b>X00</b>	
Date: Thursday, January 10, 2013		Sheet 39 of	104

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<Core Design>



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Title

**Reserved**

Size  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
OAK14 Haswell

Rev  
X00

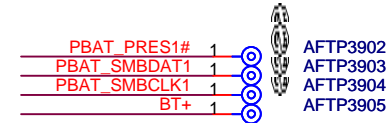
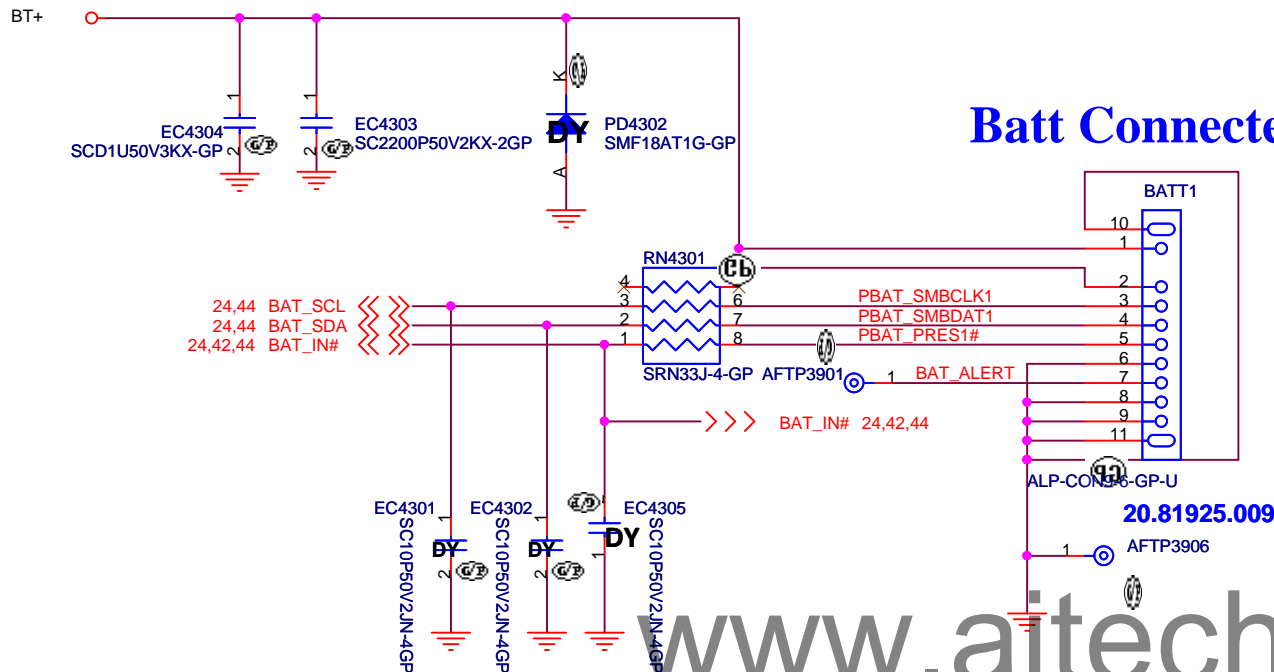
Date: Thursday, January 10, 2013

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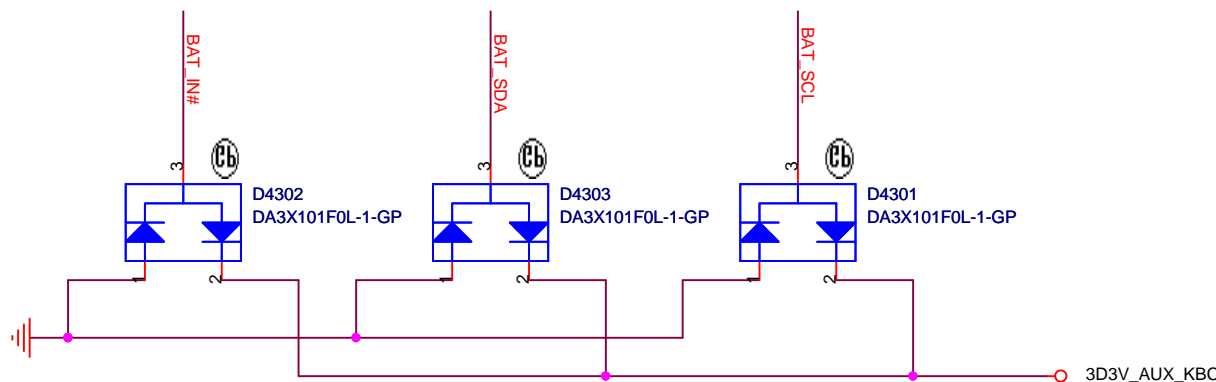
1



**SSID = PWR.Support**



Placement: Close to Batt Connector



75.03101.07D

2nd = 83.00099.K11  
3rd = 83.00099.M11

75.03101.07D

2nd = 83.00099.K11  
3rd = 83.00099.M11

75.03101.07D

2nd = 83.00099.K11  
3rd = 83.00099.M11

<Core Design>



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Title

**BATT CONN**

Size  
A4

Document Number

**OAK14 Haswell**

Rev

**X00**

Date: Thursday, March 07, 2013

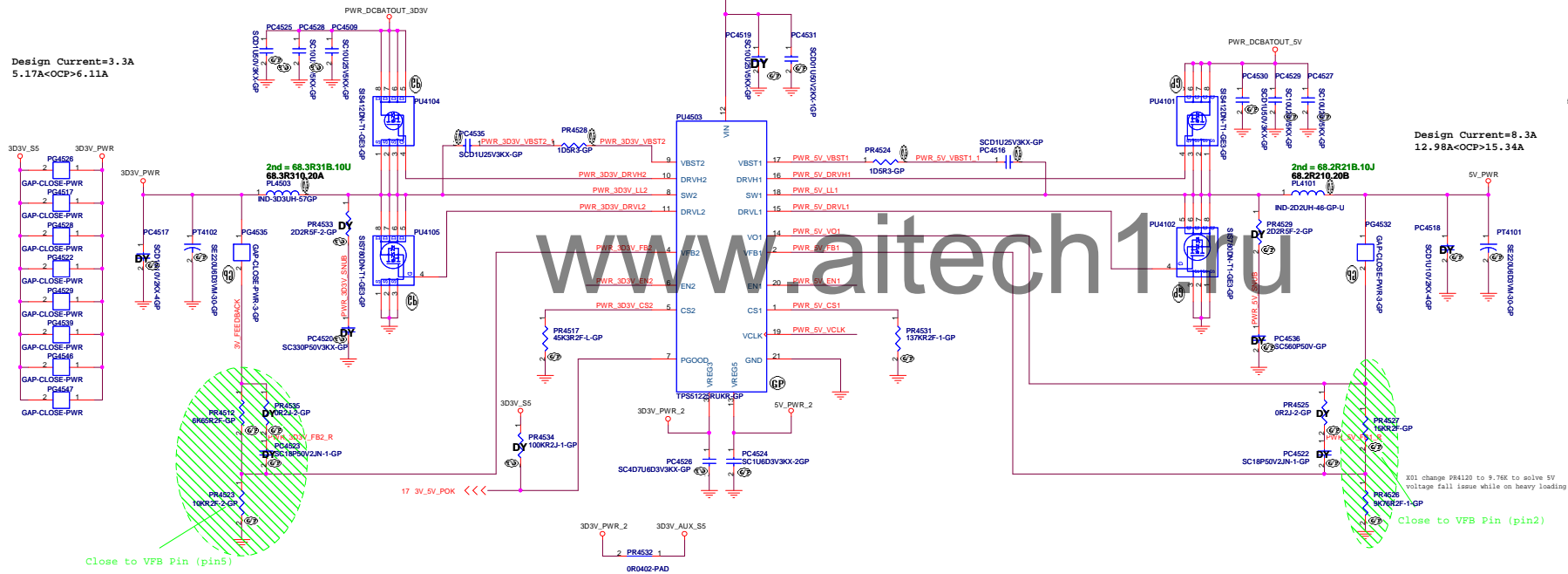
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SSID = PWR.Plane.Regulator\_5v3p3v

Design Current=3.3A  
5.17A<OCP>6.11A



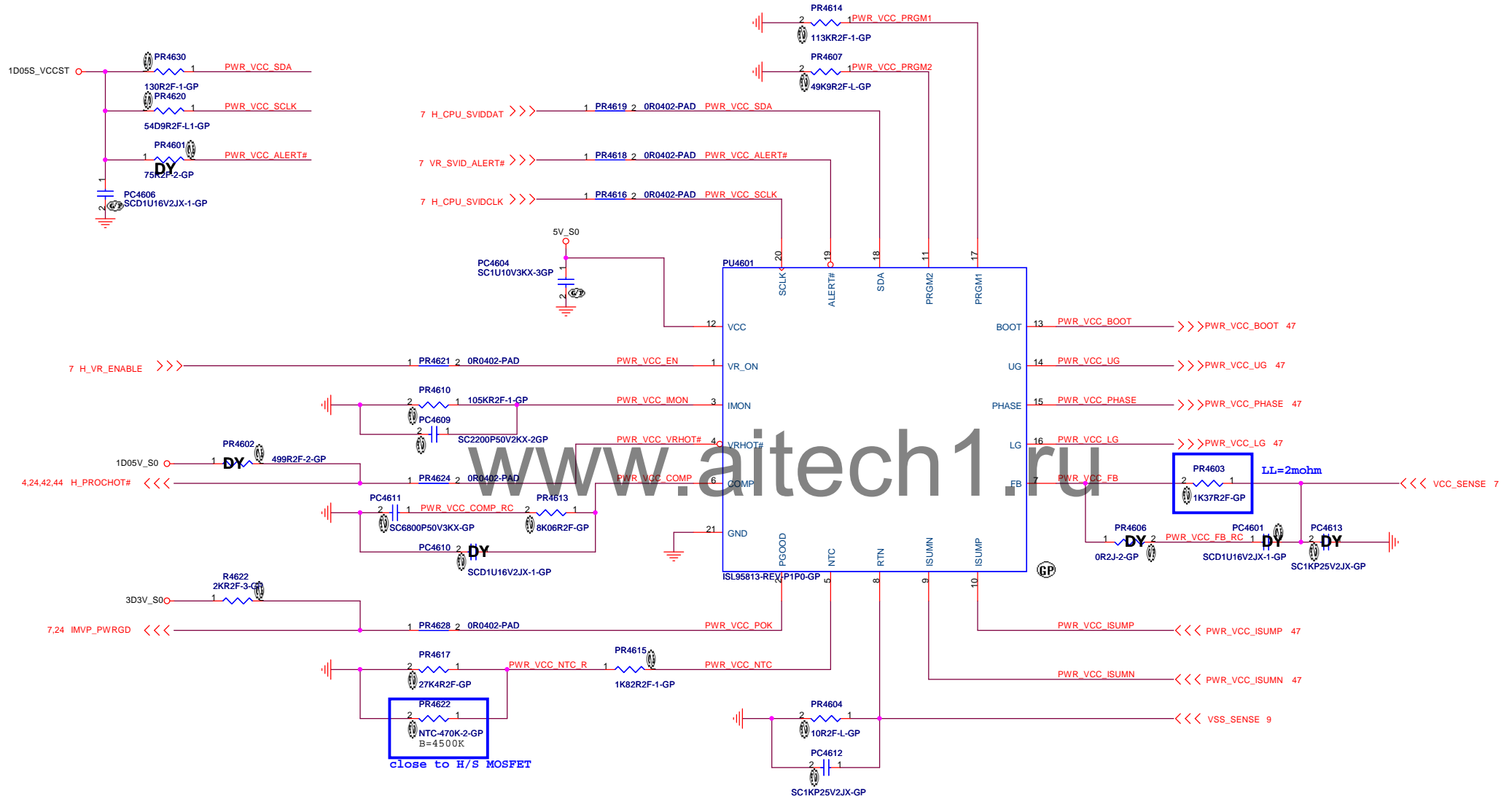
TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 2.2U PCMC063T-3R3MN Cynotec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

SSID = CPU.Regulator



<Core Design>

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Title

**TPS51622 CPUCORE(1/2)**

Size  
A3

Document Number

**OAK14 Haswell**

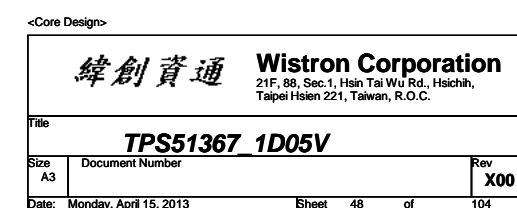
Rev  
**X00**

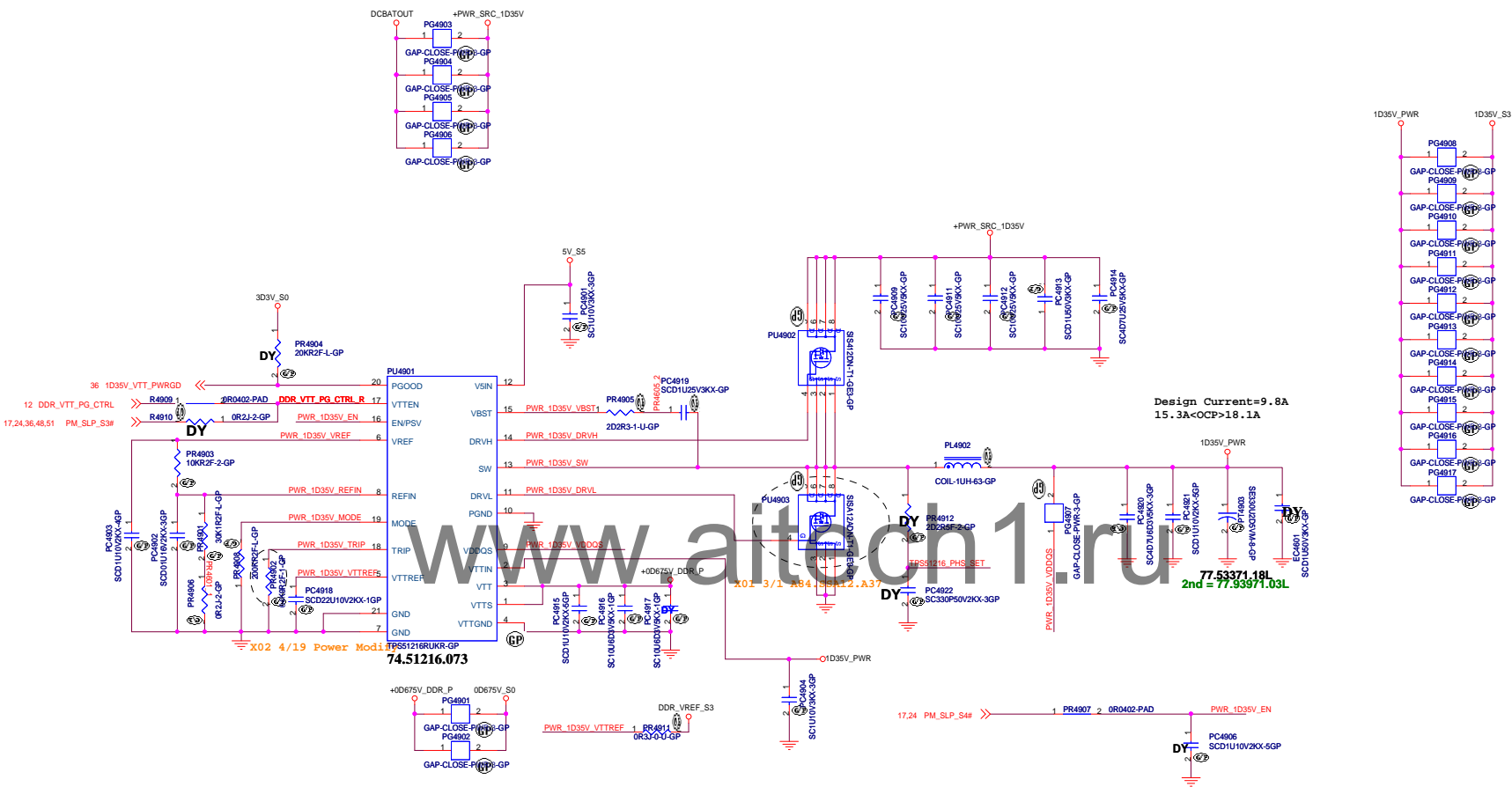
Date: Thursday, April 18, 2013

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State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T  
O/P cap: CHIP CAP POL 330U 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L  
H/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V  
L/S MOS: FET MOS SIS780DN-T1-GE3 NC POWERPAK 121 / 84.00780.037 / Rds(on)=14.5-17.5mohm @Vgs=4.5V

<Core Design>

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<Core Design>



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Title

**Reserved**

Size  
A3

Document Number

**OAK14 Haswell**

Rev

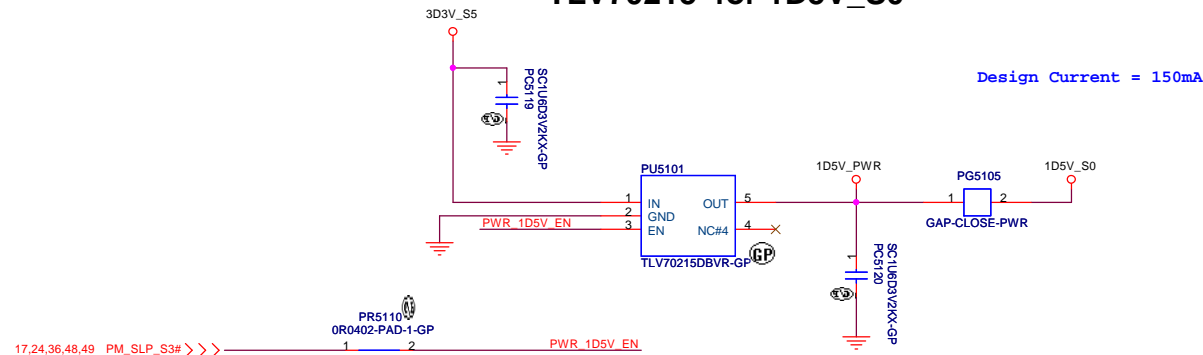
**X00**

Date: Thursday, January 10, 2013

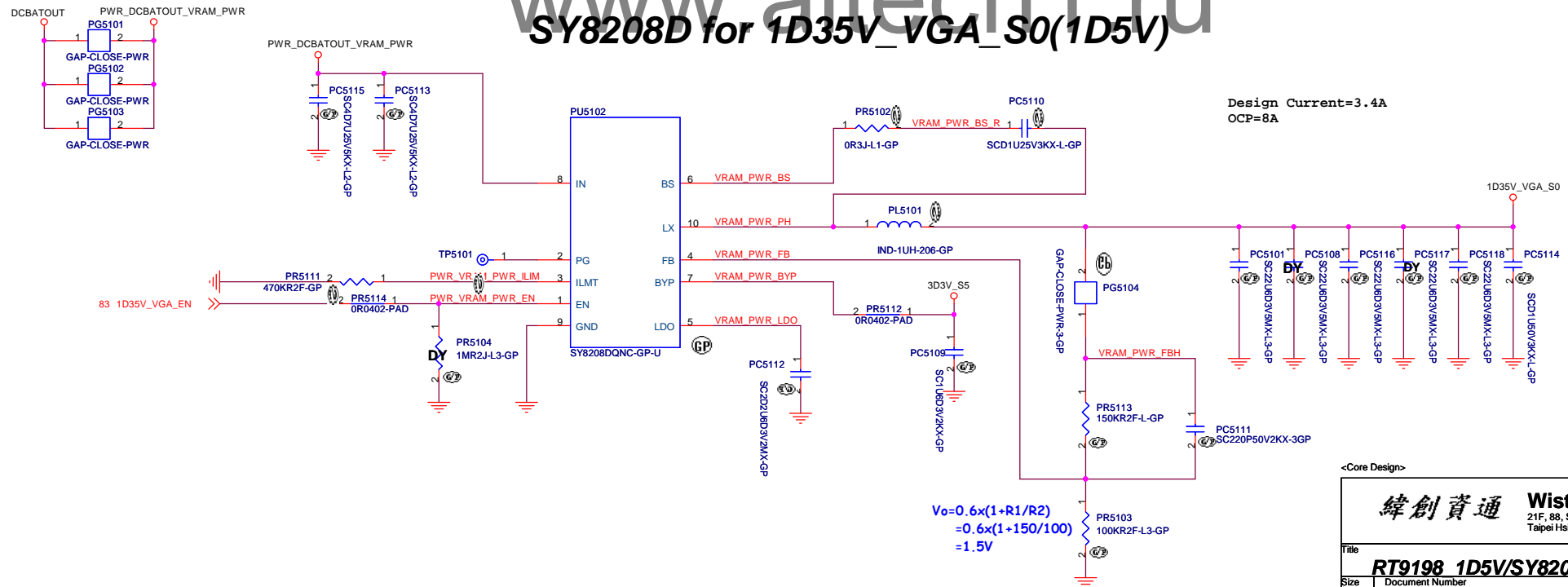
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SSID = PWR.Plane.Regulator\_1p5v

## TLV70215 for 1D5V\_S0



## SY8208D for 1D35V\_VGA\_S0(1D5V)



<Core Design>

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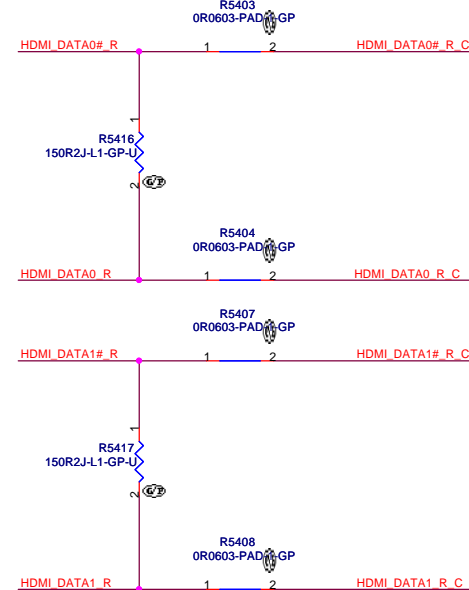
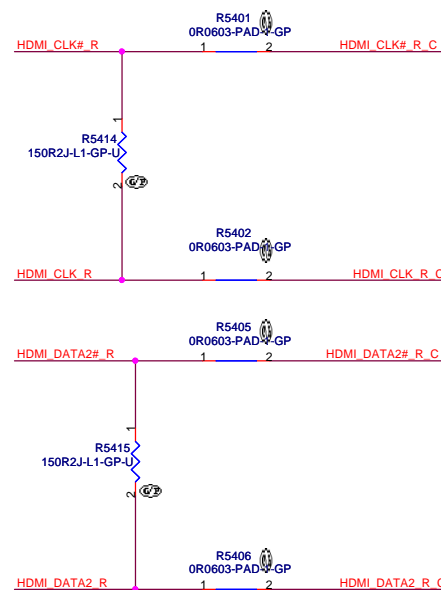
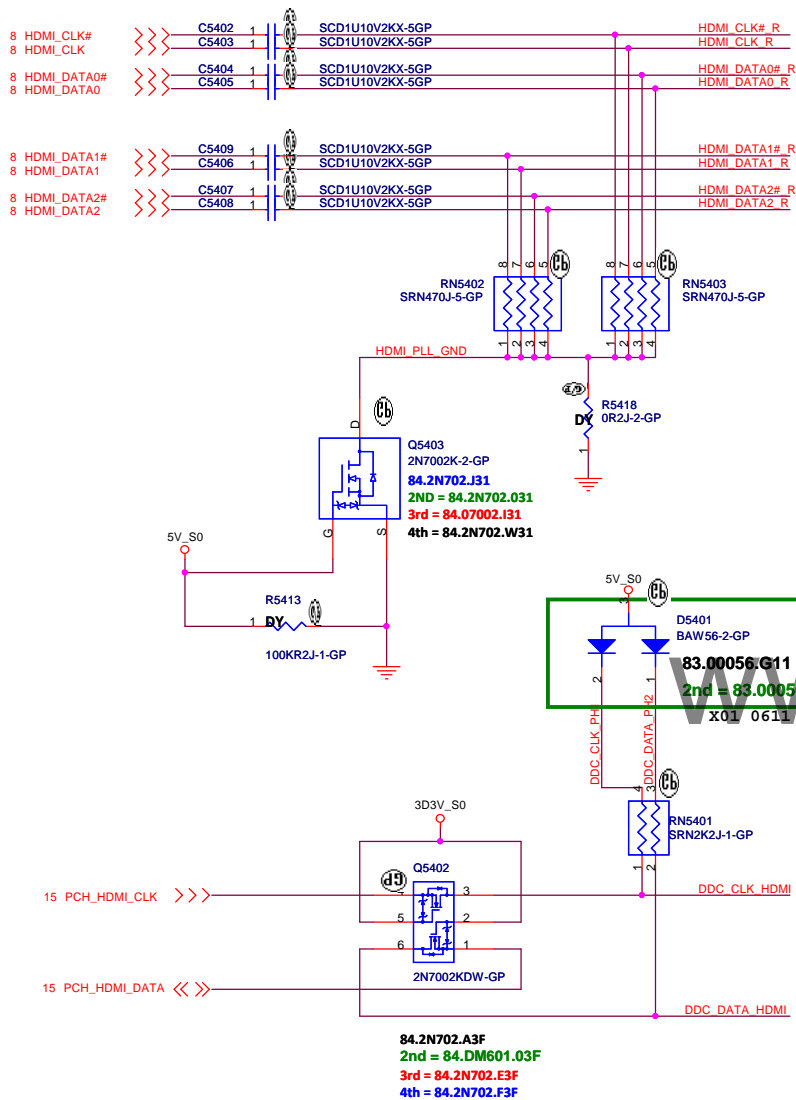
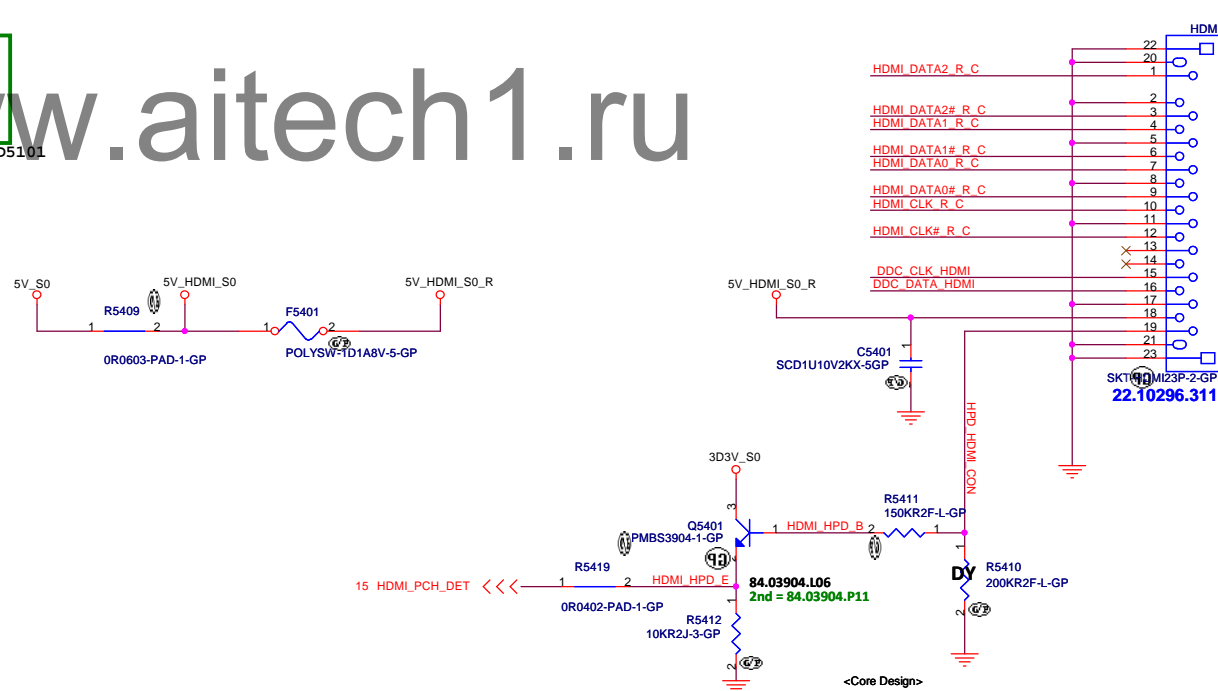
Title			RT9198 1D5V/SY8208D 1D5V(VGA)
Size	Document Number	Rev	X00
A3	OAK14 Haswell		
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## SSID = VIDEO

**HDMI CONN**

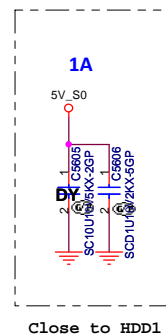
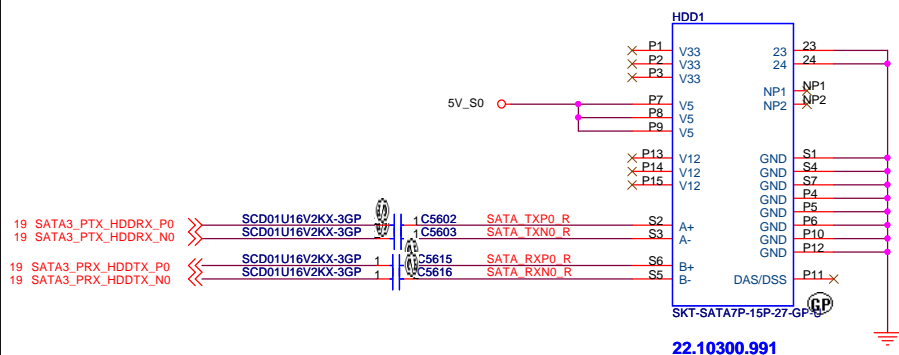
SSID = User.Interface

(Blanking)

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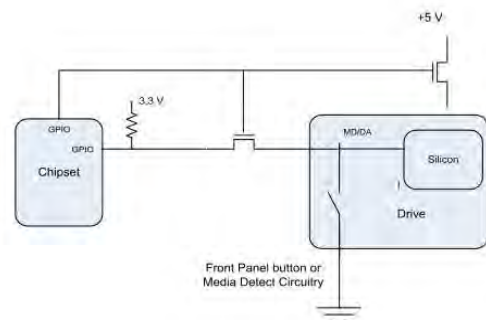
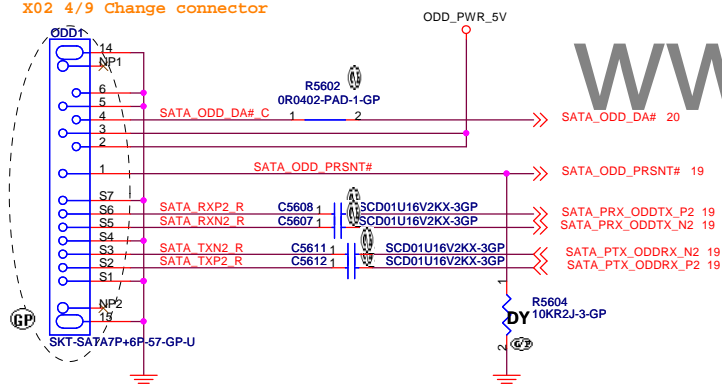
**SSID = SATA**

## SATA HDD Connector



## ODD Connector

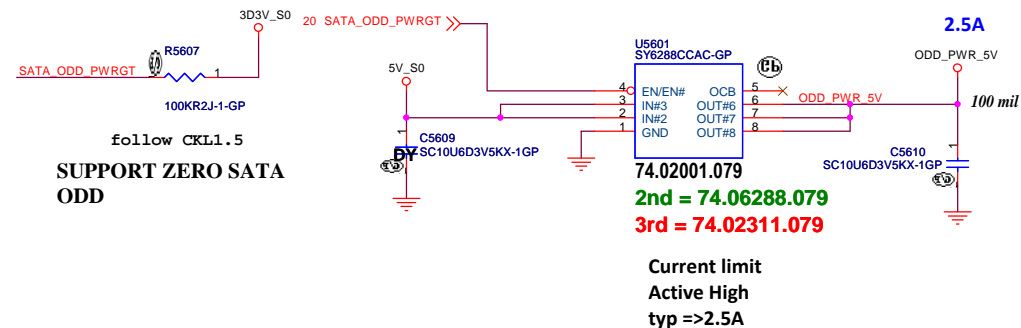
X02 4/9 Change connector



Front Panel button or Media Detect Circuitry

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## SATA Zero Power ODD



**<Core Design>**



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Title

**HDD/ODD**Size  
A3

Document Number
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SSID = ESATA

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Title

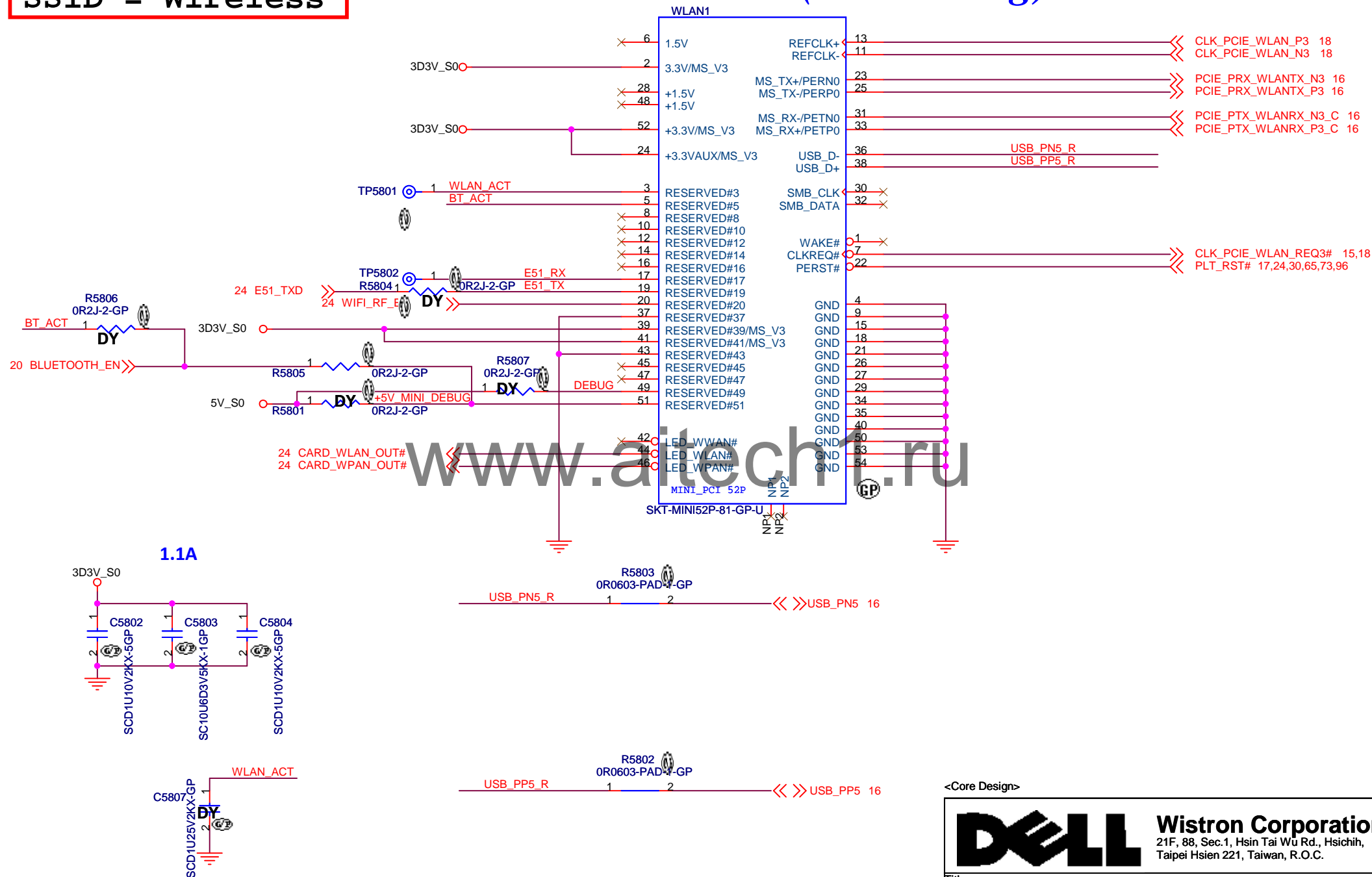
**ESATA**

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A3	<b>OAK14 Haswell</b>	<b>X00</b>

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SSID = Wireless

# Mini Card Connector(802.11a/b/g)



<Core Design>



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Title

**MINICARD(WLAN)/ITP CONN**

Size  
A4

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**OAK14 Haswell**

Rev

**X00**

Date: Thursday, April 18, 2013

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(Blanking)

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SSID = PCH

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<Core Design>

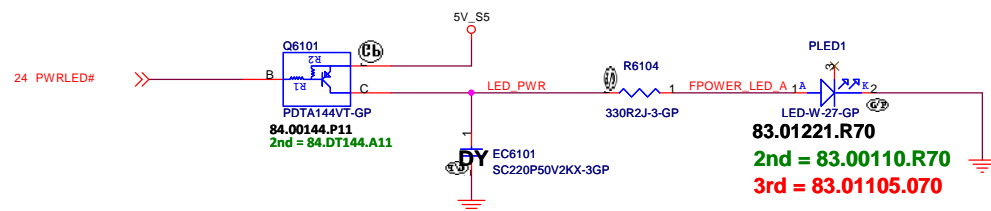


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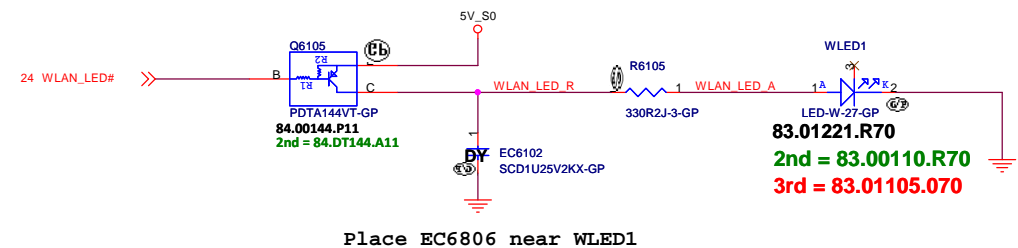
Title			(Reserved)		
Size	Document Number				Rev
A4	OAK14 Haswell				X00
Date: Thursday, January 10, 2013		Sheet 60 of		104	



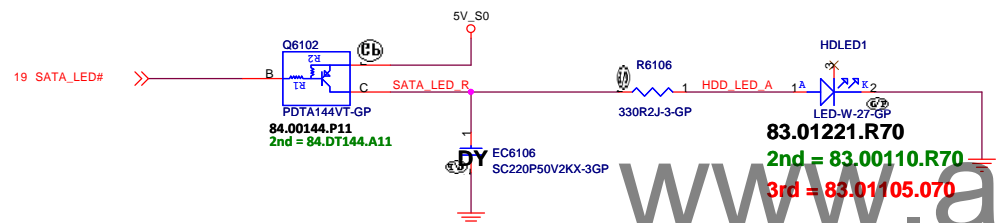
Low actived from KBC GPIO



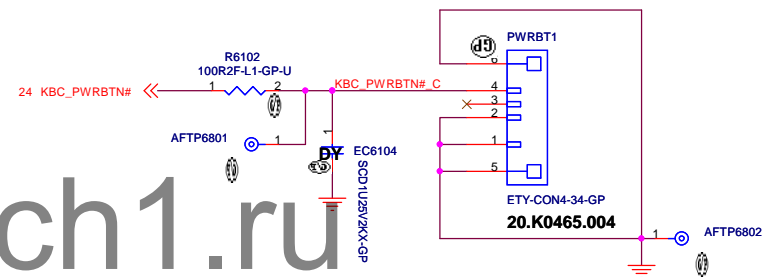
Low activated from KBC GPIO



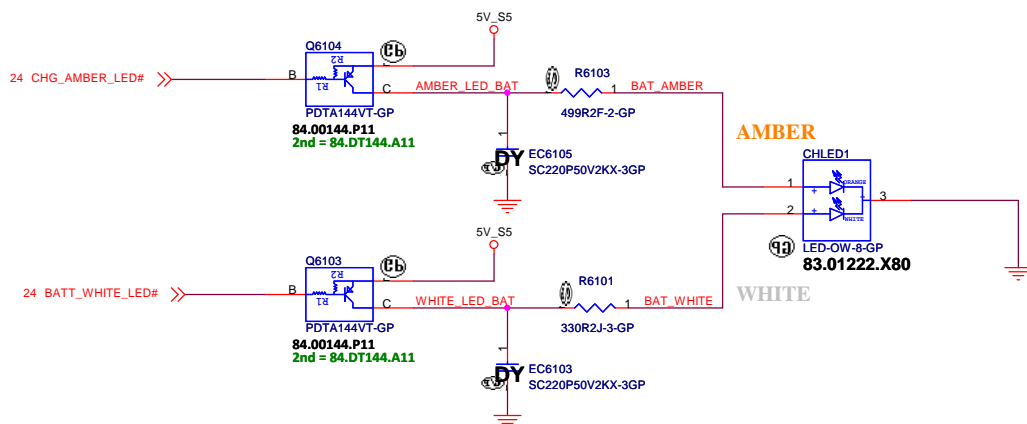
Low activated from PCH GPIO



## Power button



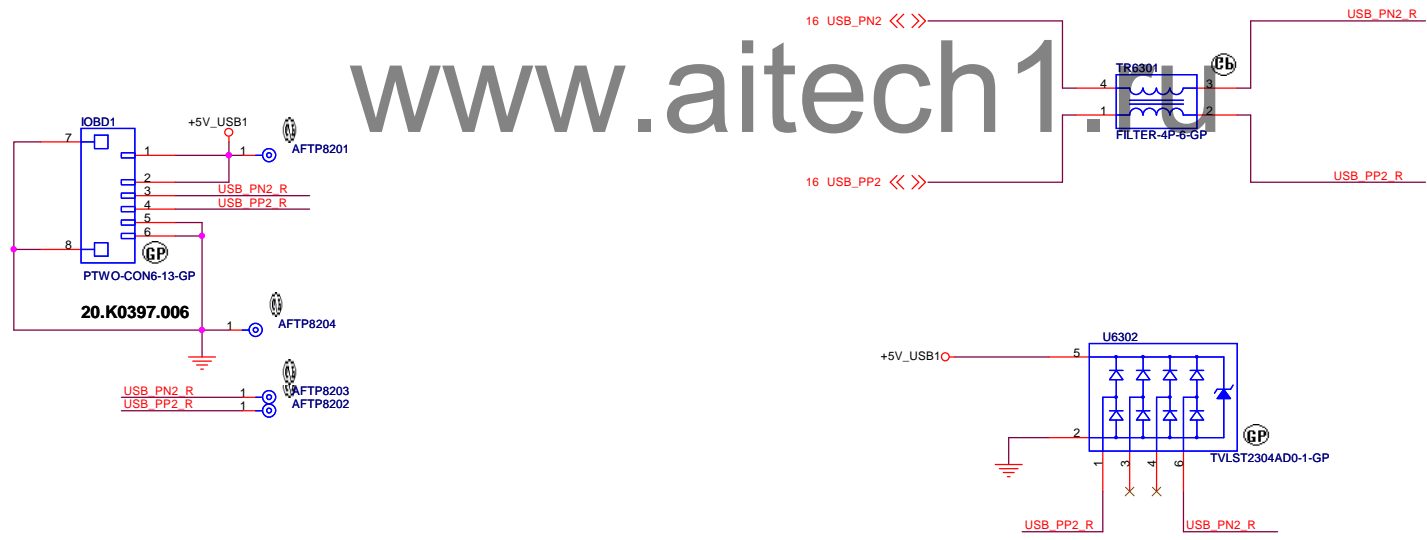
Low active from KBC GPIO



Low active from KBC GPIO



SSID = User.Interface





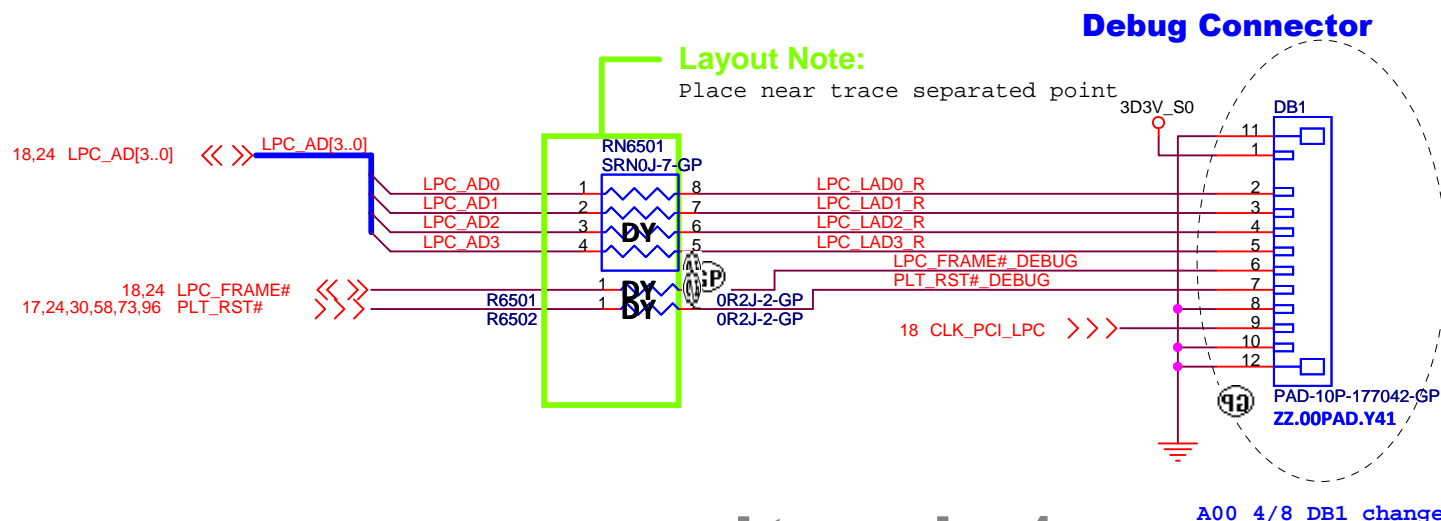
## ***Hall Sensor***

Rev  
**X00**

## OAK14 Haswell

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SSID = DEBUG PORT



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**Dubug connector**

Size  
A4

Document Number

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Rev

**X00**


Date: Monday, April 08, 2013

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Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 66 of 104
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A3	<b>OAK14 Haswell</b>	<b>X00</b>

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Size	Document Number				Rev
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Date: Thursday, January 10, 2013			Sheet	68	of 104



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**USB3.0 PORT**

Size	Document Number	Rev
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Date: Thursday, January 10, 2013

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Size  
A3

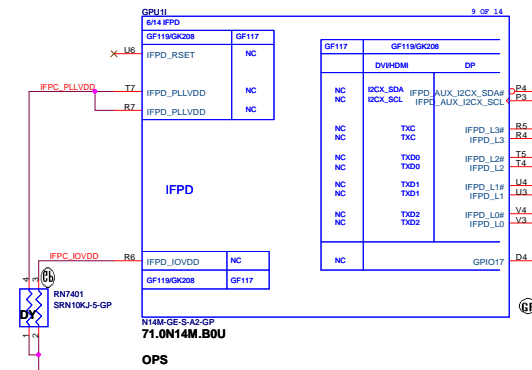
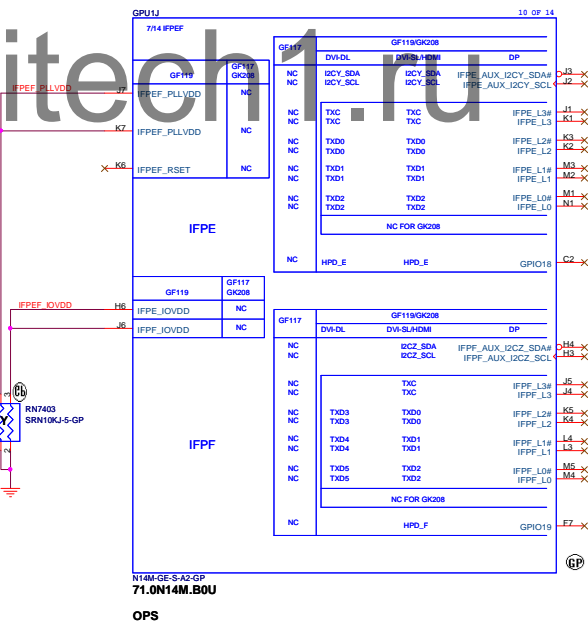
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OAK14 Haswell

Rev  
X00

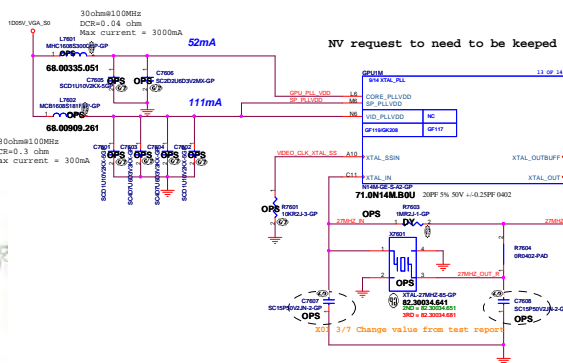
Date: Thursday, January 10, 2013Sheet 72 of 104



GPU1G		7 of 14	
		<b>GF117</b>	<b>GF118/GK208</b>
<b>GF118/GK208</b>	<b>GF117</b>	NC	IFPA_TXCH IFPA_TXC
IFPAB_RSET	NC	NC	IFPA_TXD0H IFPA_TXD0
IFPAB_PLLVDD	NC	NC	IFPA_TXD1H IFPA_TXD1
IFPAB_PLLVDD	NC	NC	IFPA_TXD2H IFPA_TXD2
		NC	IFPA_TXD3H IFPA_TXD3
		NC	IFPB_TXCH IFPB_TXC
<b>GF118/GK208</b>	<b>GF117</b>	NC	IFPB_TXD4H IFPB_TXD4
IFPBA_IOVDD	NC	NC	IFPB_TXD5H IFPB_TXD5
IFPBA_IOVDD	NC	NC	IFPB_TXD6H IFPB_TXD6
		NC	IFPB_TXD7H IFPB_TXD7
		NC	GPIO14
<b>IIFPAB</b>			
N1M4GE-S-A2-GP			
<b>71.0N14M.BOU</b>			

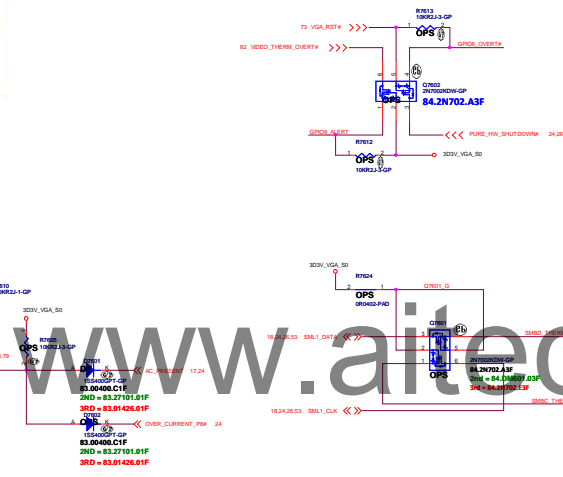
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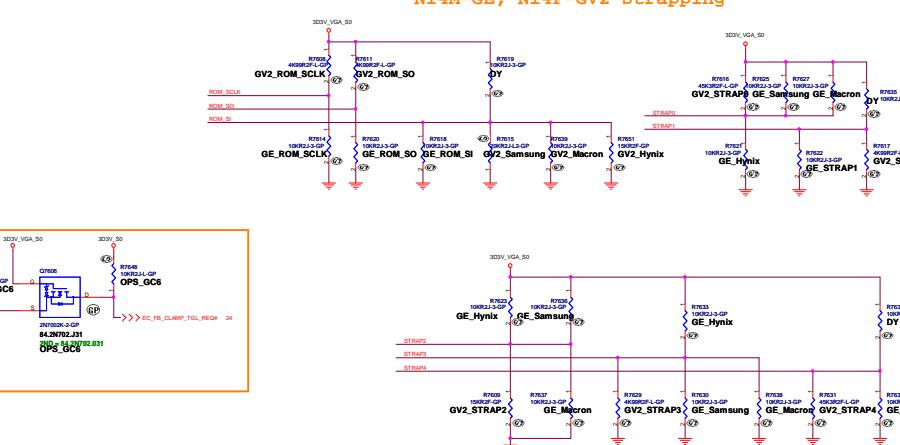


NV request to need to be keeped

Table 113. GB2-64, GB4-128, GB2-192 and GB3-256 PLL Power Rail Filter - SP, PLLVDD and VID, PLLVDD Combined

[illegible]

## N14M-GE, N14P-GV2 Strapping



Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
128M*16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-09G-K	1000	1234	Production ready
				MT41J128M16JT-107G-K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4V2G1644E-BC1A	1000	1204	Production ready
				K4V2G1644E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-110C	1000	11/A	Production ready
				H5TQ2G63DFR-11C	900	11/A	Production ready
		0xC	1.5V/ 1.5V	H5TC2G63FR-11C	1000	11/A	Post production candidate

Configuration	Vendor	Strap	FBVDD/ FBIDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
Z56Aa16 D0R3	Saionius	0x3	1.5 V/ 1.5 V	K4W9K16A08-HC11	900	11/A	Production ready
	Allicon	0xc1	1.5 V/ 1.5 V	MT41K256M16A1A-107C-E	900	11/A	Production ready
	Hynix	0xc2	1.5V/ 1.5V	H5TC4G634FR-11C	900	11/A	Production ready

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SEL	SUB_ADDR	10k Ω	Pull-down to GND
ROM_S	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists. Pull-down to GND if no VBIOS ROM
ROM_S0	VEGA_DEVICE	10k Ω	Pull-down to GND (not always)
ROM_CFG0	RAM_CFG0	10k Ω	See RAM below
STRAP1	RAM_CFG1	10k Ω	See Hiccup below
STRAP2	RAM_CFG2	10k Ω	See Hiccup below
STRAP3	RAM_CFG3	10k Ω	See Hiccup below
STRAP4	PROC_MAX_SPEED	10k Ω	Pull-down to GND

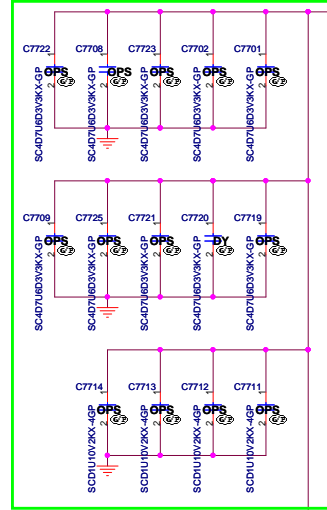
	N14M-LP	N14M-GS	N14P-GV	N14P-GV2
Chip Part #	GK208-640 (Small package)	GK208-630 (Small package)	GK208-650 (Small package)	GK208-632 (Small package)
	GK208-740 (Big package)	GK208-730 (Big package)	GK208-750 (Big package)	GK208-732 (Big package)
Device ID	0x1291	0x1290	0x1294	0x1292

Group (Pilot name)	Original of training from SHER	Original of training from SHER	Original of training from SHER	Original of training from SHER
	from PRACTICE	from PRACTICE	from PRACTICE	from PRACTICE
ROM 10	1	0	0	0
ROM 11	0	0	0	1
ROM 20	0	0	0	0
ROM 21	0	0	0	0
ROM 30	0	0	0	0
ROM 31	0	0	0	0
ROM 40	0	0	0	0
ROM 41	0	0	0	0
ROM 50	0	0	0	0
ROM 51	0	0	0	0
ROM 60	0	0	0	0
ROM 61	0	0	0	0
ROM 70	0	0	0	0
ROM 71	0	0	0	0
ROM 80	0	0	0	0
ROM 81	0	0	0	0
ROM 90	0	0	0	0
ROM 91	0	0	0	0
ROM 100	0	0	0	0
ROM 101	0	0	0	0
ROM 110	0	0	0	0
ROM 111	0	0	0	0
ROM 120	0	0	0	0
ROM 121	0	0	0	0
ROM 130	0	0	0	0
ROM 131	0	0	0	0
ROM 140	0	0	0	0
ROM 141	0	0	0	0
ROM 150	0	0	0	0
ROM 151	0	0	0	0
ROM 160	0	0	0	0
ROM 161	0	0	0	0
ROM 170	0	0	0	0
ROM 171	0	0	0	0
ROM 180	0	0	0	0
ROM 181	0	0	0	0
ROM 190	0	0	0	0
ROM 191	0	0	0	0
ROM 200	0	0	0	0
ROM 201	0	0	0	0
ROM 210	0	0	0	0
ROM 211	0	0	0	0
ROM 220	0	0	0	0
ROM 221	0	0	0	0
ROM 230	0	0	0	0
ROM 231	0	0	0	0
ROM 240	0	0	0	0
ROM 241	0	0	0	0
ROM 250	0	0	0	0
ROM 251	0	0	0	0
ROM 260	0	0	0	0
ROM 261	0	0	0	0
ROM 270	0	0	0	0
ROM 271	0	0	0	0
ROM 280	0	0	0	0
ROM 281	0	0	0	0
ROM 290	0	0	0	0
ROM 291	0	0	0	0
ROM 300	0	0	0	0
ROM 301	0	0	0	0
ROM 310	0	0	0	0
ROM 311	0	0	0	0
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ROM 321	0	0	0	0
ROM 330	0	0	0	0
ROM 331	0	0	0	0
ROM 340	0	0	0	0
ROM 341	0	0	0	0
ROM 350	0	0	0	0
ROM 351	0	0	0	0
ROM 360	0	0	0	0
ROM 361	0	0	0	0
ROM 370	0	0	0	0
ROM 371	0	0	0	0
ROM 380	0	0	0	0
ROM 381	0	0	0	0
ROM 390	0	0	0	0
ROM 391	0	0	0	0
ROM 400	0	0	0	0
ROM 401	0	0	0	0
ROM 410	0	0	0	0
ROM 411	0	0	0	0
ROM 420	0	0	0	0
ROM 421	0	0	0	0
ROM 430	0	0	0	0
ROM 431	0	0	0	0
ROM 440	0	0	0	0
ROM 441	0	0	0	0
ROM 450	0	0	0	0
ROM 451	0	0	0	0
ROM 460	0	0	0	0
ROM 461	0	0	0	0
ROM 470	0	0	0	0
ROM 471	0	0	0	0
ROM 480	0	0	0	0
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ROM 490	0	0	0	0
ROM 491	0	0	0	0
ROM 500	0	0	0	0
ROM 501	0	0	0	0

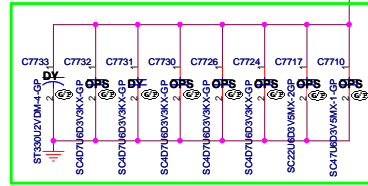
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# Under GPU

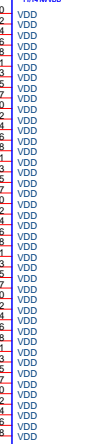


# Near GPU



VGA\_CORE

GPU1E 5 OF 14

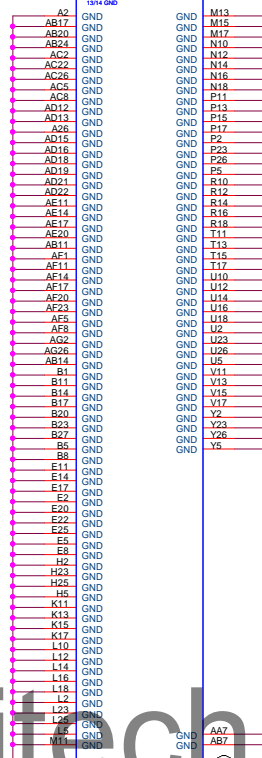


N14M-GE-S-A2-GP

71.0N14M.B0U

OPS

GPU1F 6 OF 14

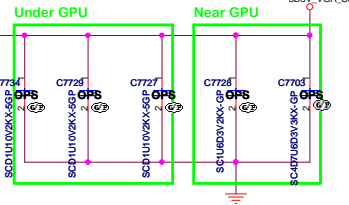


N14M-GE-S-A2-GP

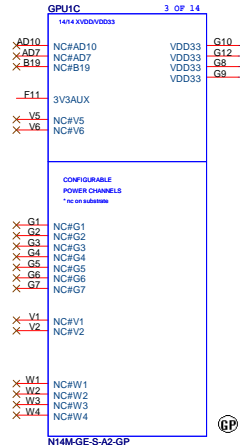
71.0N14M.B0U

OPS

3.3V +/- 5%  
85mA



3D3V\_VGA\_S0



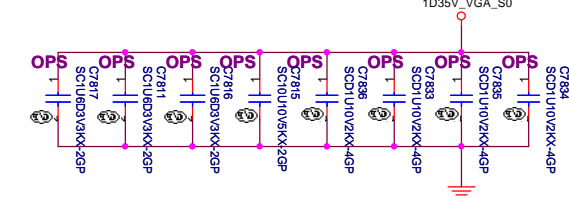
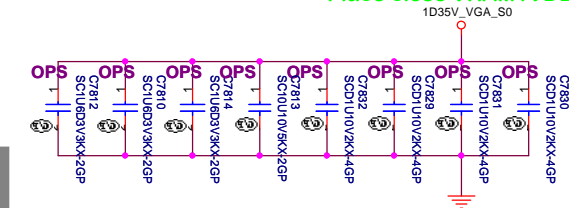
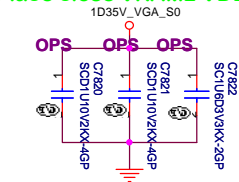
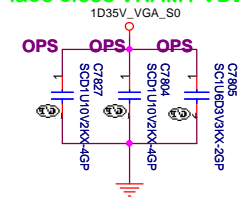
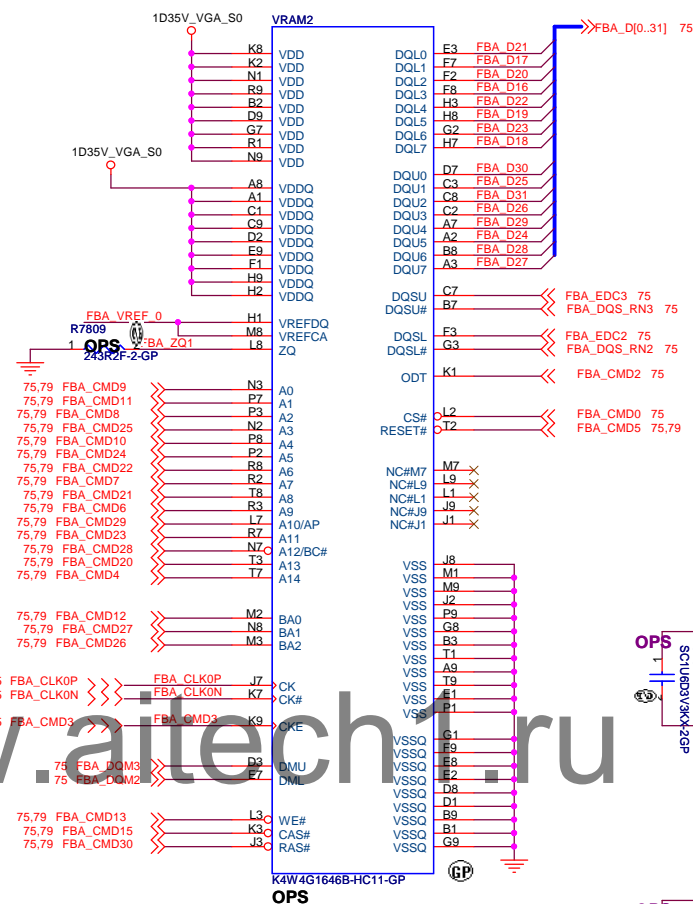
N14M-GE-S-A2-GP

71.0N14M.B0U

OPS

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<b>DELL</b>		<b>Wistron Corporation</b>	
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Title: <b>GPU DPPWR/GND(5/5)</b>			
Size: Custom	Document Number: <b>OAK14 Haswell</b>	Rev: <b>X00</b>	
Date: Friday, April 19, 2013	Sheet: 77	of	104



1D35V\_VGA\_S0

R7805 1K392F-GP

OPS

FBA\_VREF\_0

C7805

OPS

R7807 1K392F-GP

R7804 S878F-A-GP

FBA\_VREF\_FET\_L

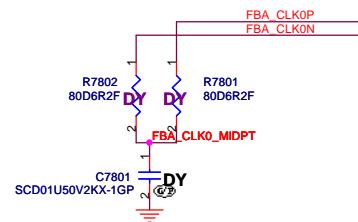
Q7801 2N7002K-2-GP

84.2N702.J31

2ND = 84.2N702.031

Description

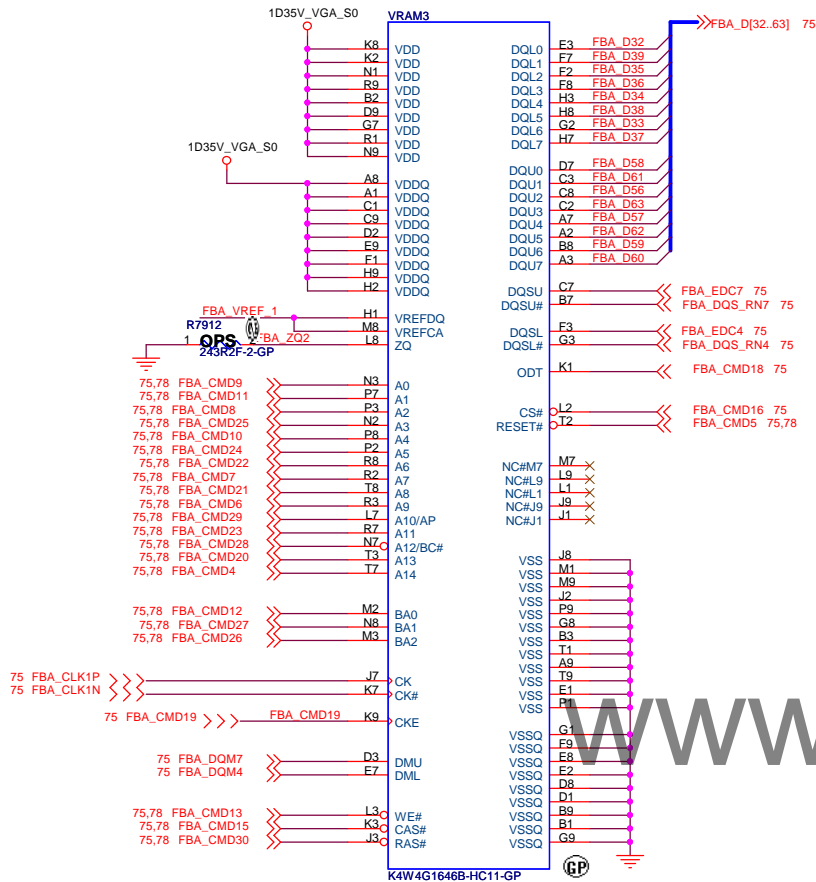
GPI010\_FBVREF >>>



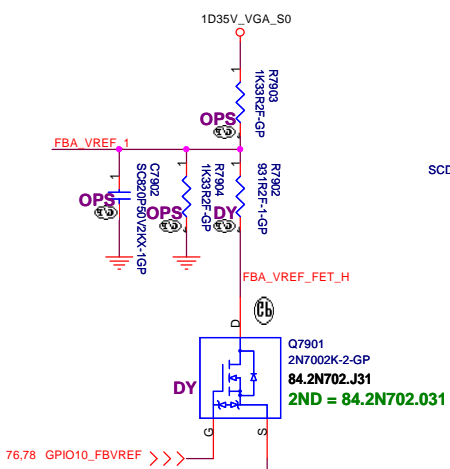
**R7810**  
162R2F-GP  
**OPS**

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

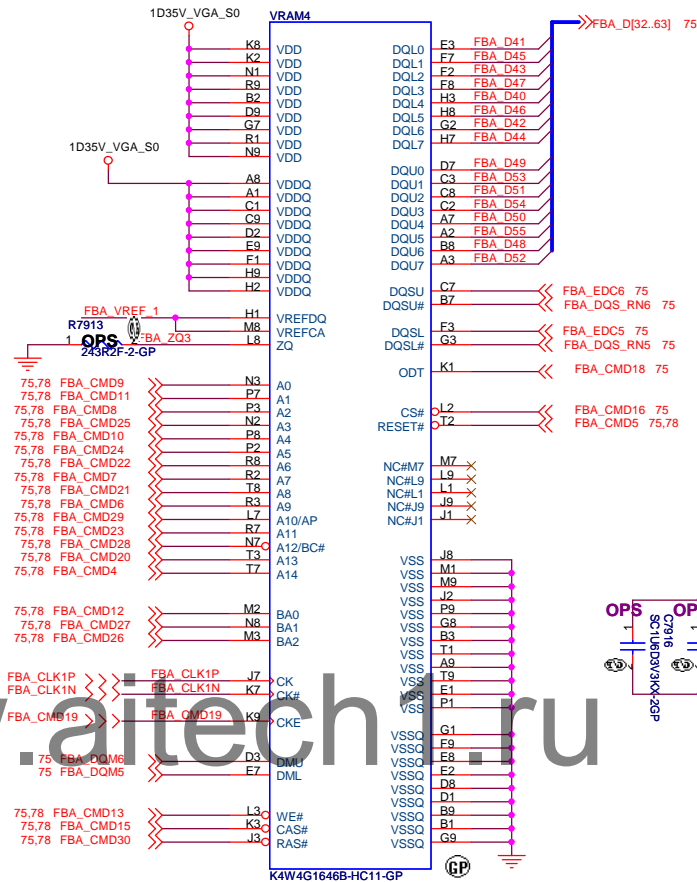
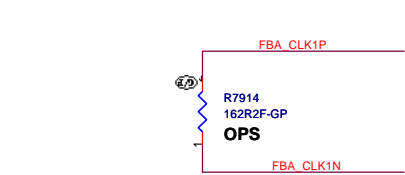
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU-VRAM1,2 (1/4)</b>			
Size A3	Document Number	Rev	
<b>OAK14 Haswell</b>		<b>X000</b>	
Date:	Wednesday, April 17, 2013	Sheet	78 of 104



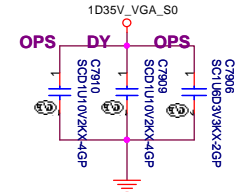
**Frame Buffer Partition A-Lower Half**



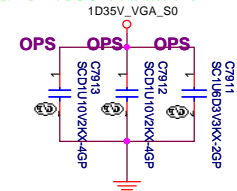
**FBCLK Termination place on VRAM side**



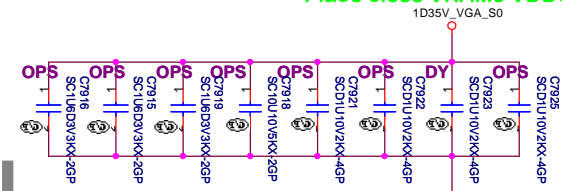
**Place close VRAM3 VDD ball**



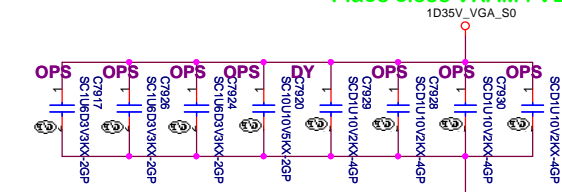
**Place close VRAM4 VDD ball**



**Place close VRAM3 VDDQ ball**




**Place close VRAM4 VDDQ ball**



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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

Size

A3

Document Number

OAK14 Haswell

Rev

X00

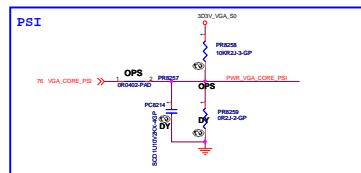
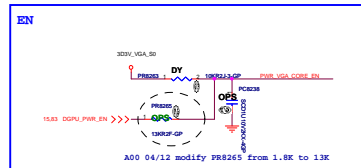
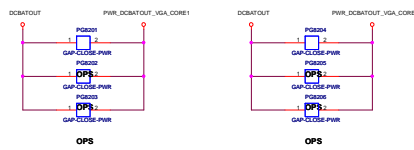
Date: Thursday, January 10, 2013

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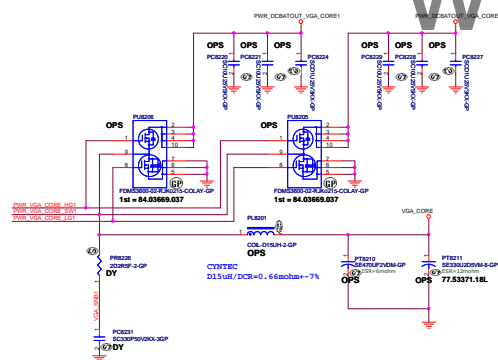
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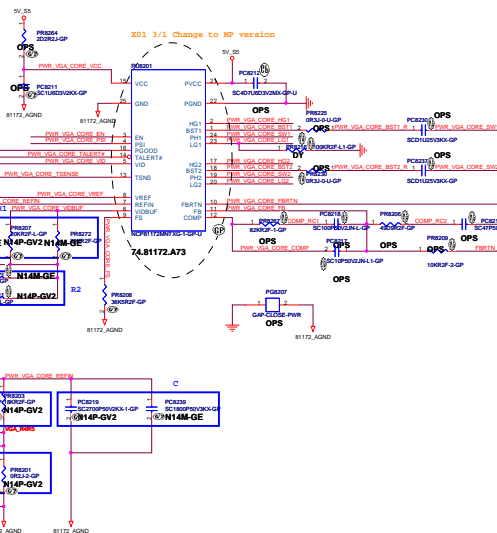
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Title			
GPU-VRAM7,8 (4/4)			
Size A3	Document Number		Rev
	OAK14 Haswell		X00
Date: Thursday, January 10, 2013		Sheet	81 of 104



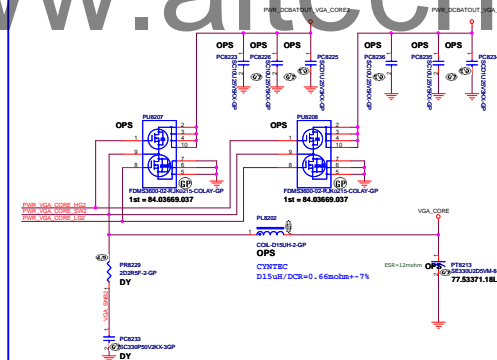
Phase1



I/P cap: 100 25V K8005 XSR/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mOhm / Q2: Id=17A, Rds(on)=3.6-5.2mOhm 84.03669.037  
 Inductor: CHIP CHOKER 0.22mH PCB060637-R22MS 2.5-3mOhm Isat =34Arms 68.82210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsui/77.53371.18L



Phase2



I/P cap: 100 25V K8005 XSR/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mOhm / Q2: Id=17A, Rds(on)=3.6-5.2mOhm 84.03669.037  
 Inductor: CHIP CHOKER 0.22mH PCB060637-R22MS 2.5-3mOhm Isat =34Arms 68.82210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsui/77.53371.18L

EDC=45A  
 EDP=72A

TYPE	config	TDC	SDP	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14M-GE	C	35A	41A		39kohm	30kohm	3kohm	24kohm	3kohm	1.8nF
N14P-GV2	B	32A	55A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF
N14P-GT	B	45A	75A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF

Table 1. PWM-VID Spec and Component Values

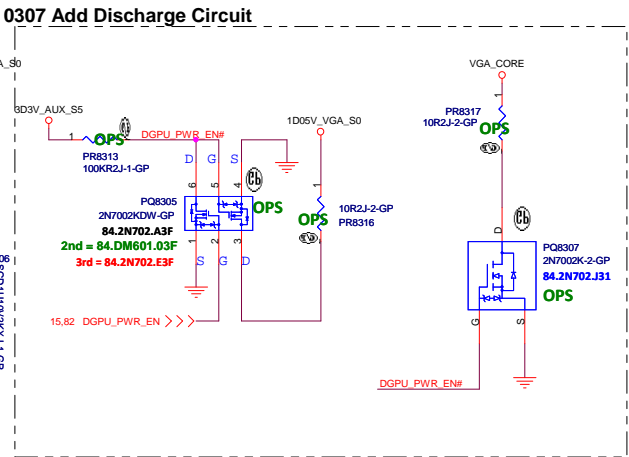
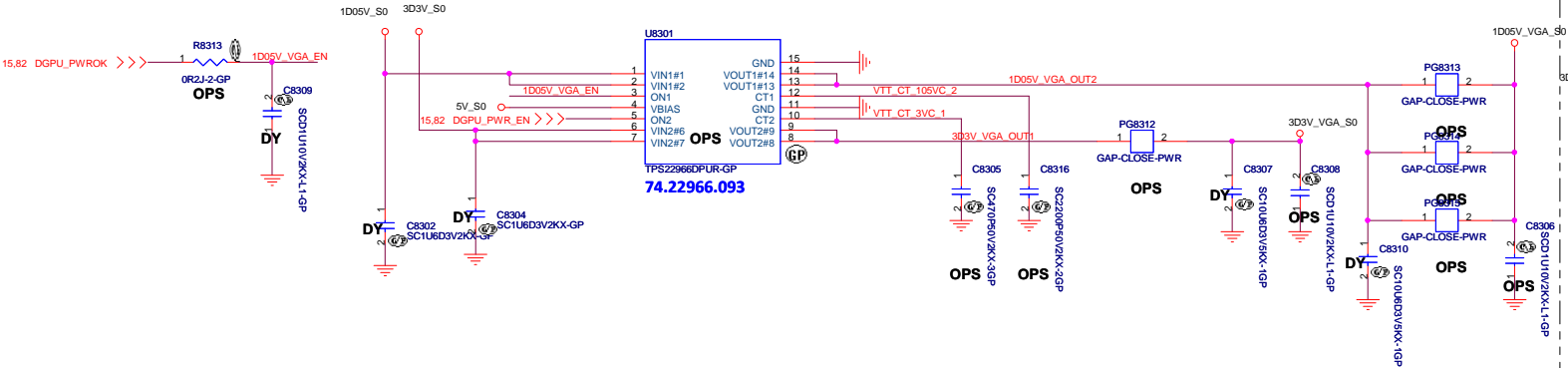
PWM-VID Spec	Config A	Config B	Config C
Vmin	V 0.6	0.6	0.65
Vmax	V 1.2	1.2	1.15
Vboot	V 0.875	0.9	0.9
Voltage Step-Vstep	mV 6.25	6.25	3.5
Number of Voltage Levels N	level 96	96	20
PWM Frequency F <sub>sw</sub>	Hz 1.125	1.125	0.676
Pulse Minimum Pulse Width T <sub>min</sub>	ns 9.26	9.26	74
VID Transient Time T	us <100	<100	<100
Component Value			
R1 (1%)	KΩ 30	20	30
R2 (1%)	KΩ 30	20	30
R3 (1%)	KΩ 1.5	2	3
R4 (1%)	KΩ 30	18	24
R5 (1%)	KΩ 1.5	0	3
C	nF 1.5	2.7	1.8

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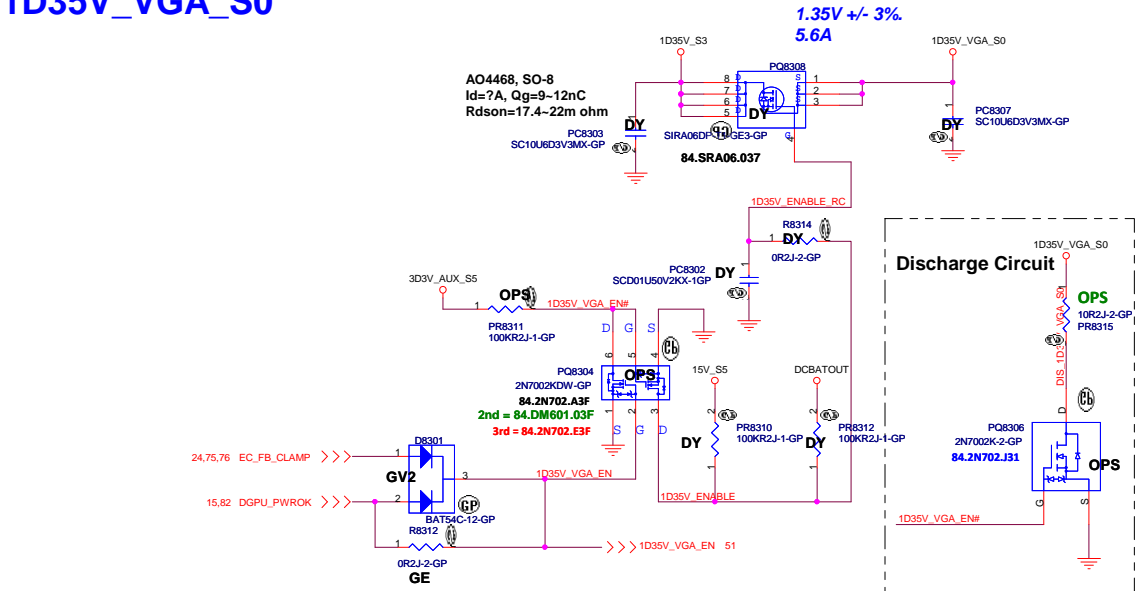
3D3V\_VGA\_S0  
1D05V\_VGA\_S0

3D3V\_VGA\_S0 should ramp-up before VGA\_Core  
VGA\_Core should ramp-up before 1D5V\_VGA\_S0  
1D35V\_VGA\_S0 should ramp-up before 1D05V\_VGA\_S0

3D3V\_S0 to 3D3V\_VGA\_S0  
1D05V\_S0 to 1D05V\_VGA\_S0



1D35V\_VGA\_S0



C <sub>Tx</sub> (pF)	Rise Time (μs) 10% - 90%, C <sub>OUT</sub> = 0.1μF @ VIN; V <sub>OUT</sub> = 0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. C<sub>Tx</sub> value

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DISCRETE VGA POWER

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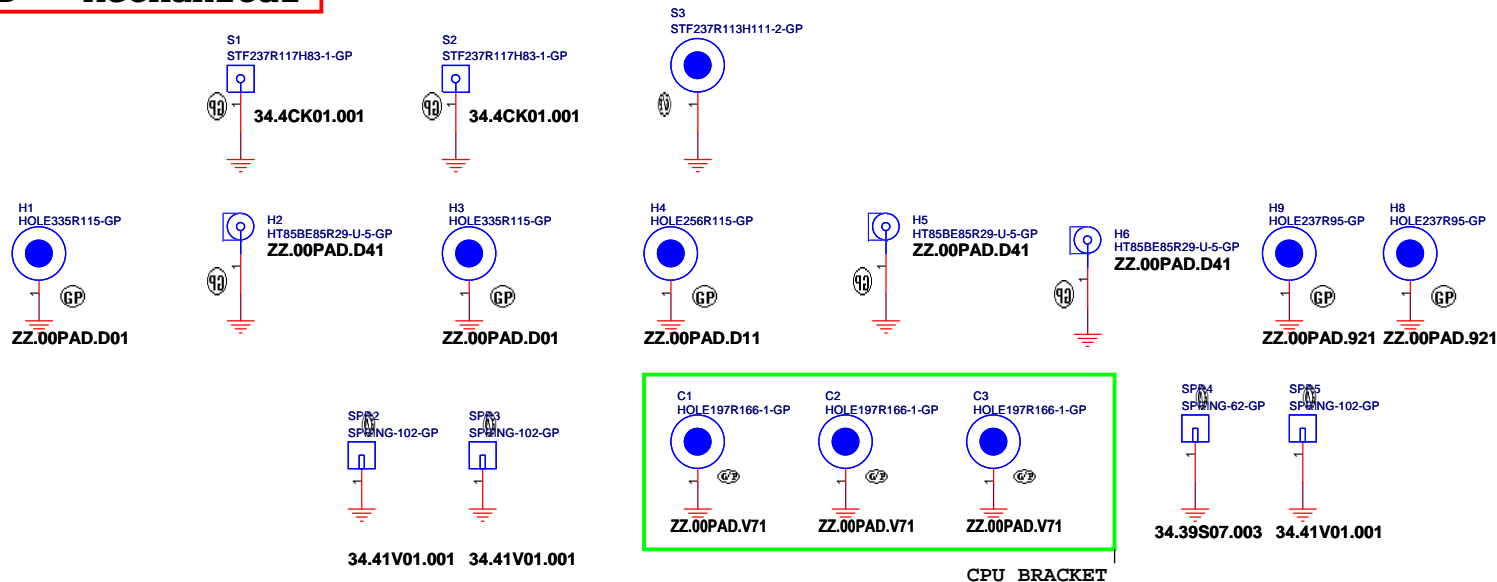
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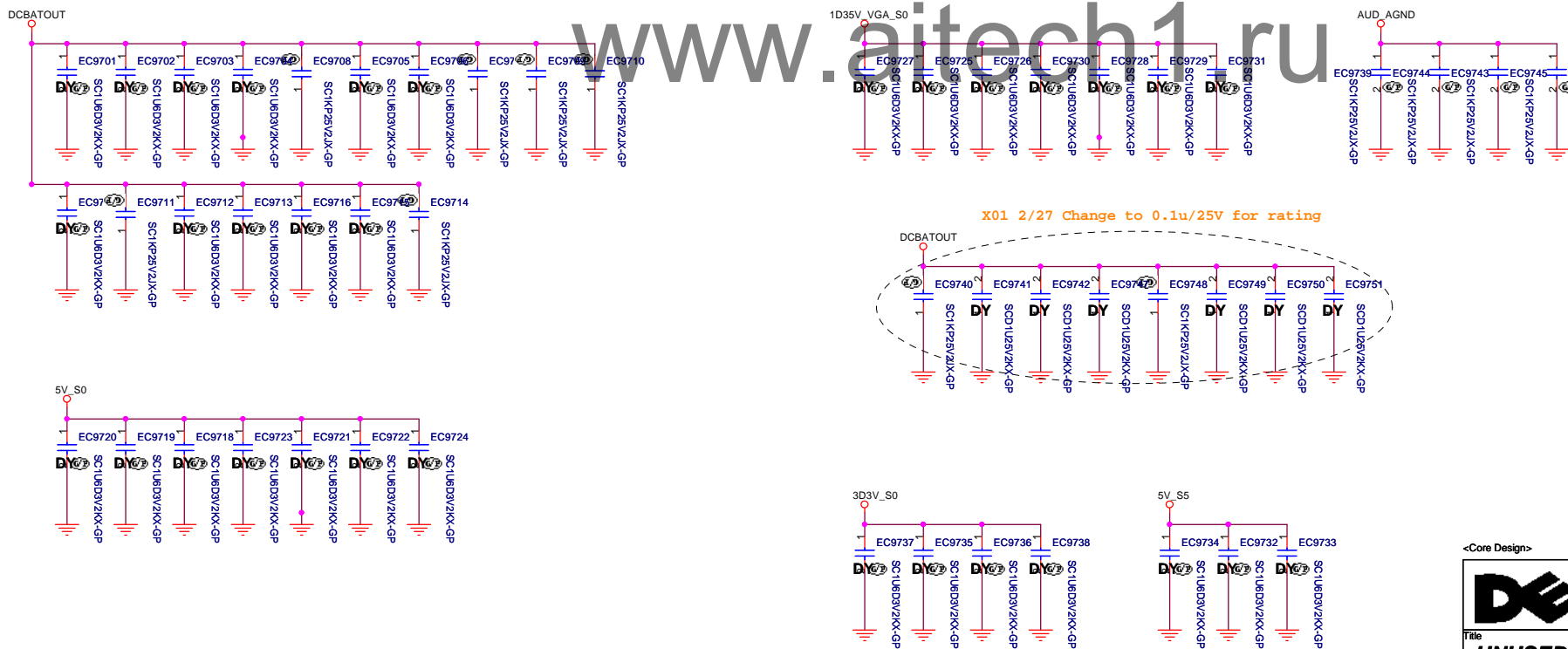
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# SSID = Mechanical



# SSID = EMI



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***Free Fall Sensor***

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**Express Card**

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LVDS Switch

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CRT Switch

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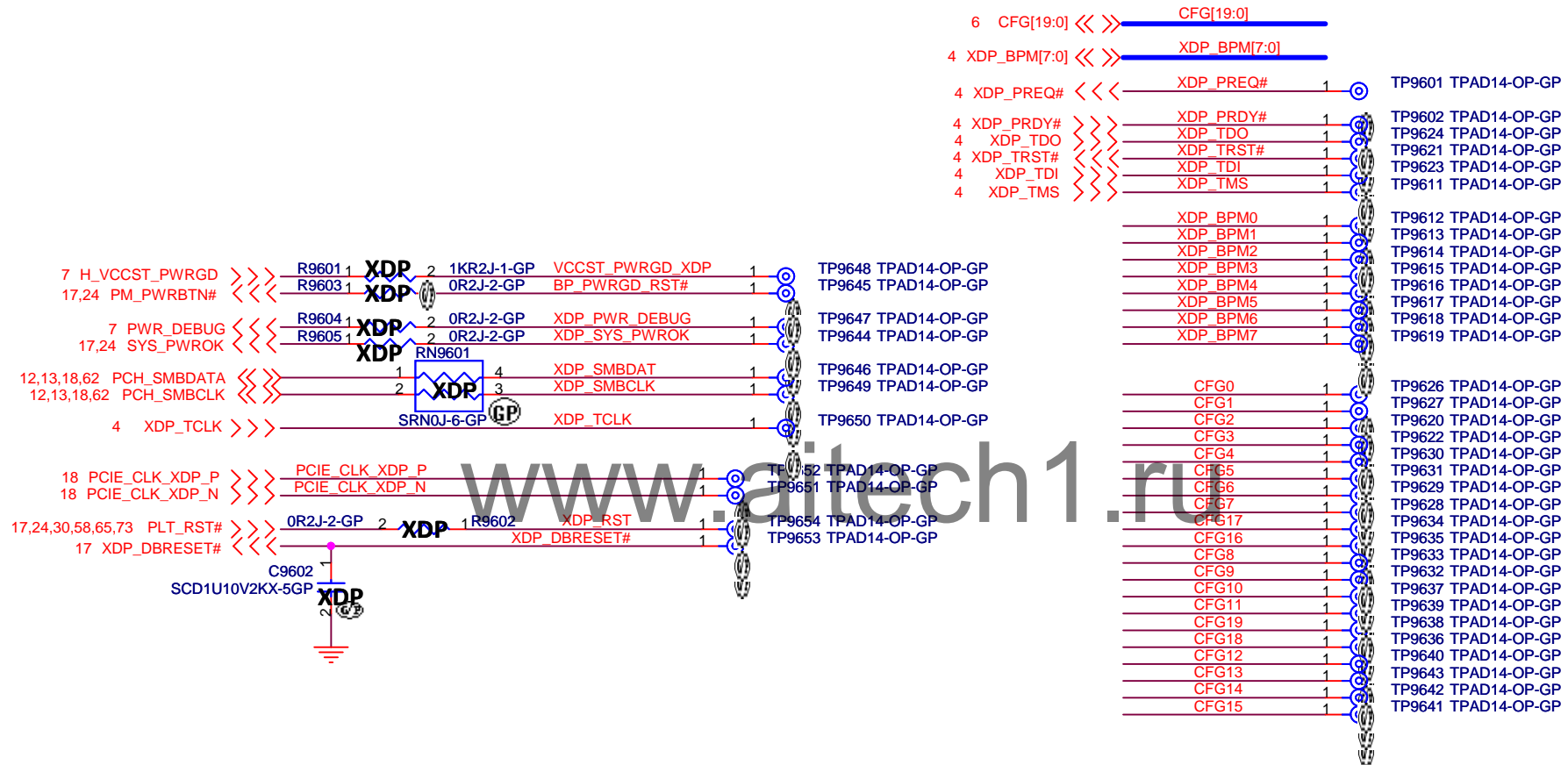
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SSID = XDP

## CPU XDP



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**TOUCH PANEL**

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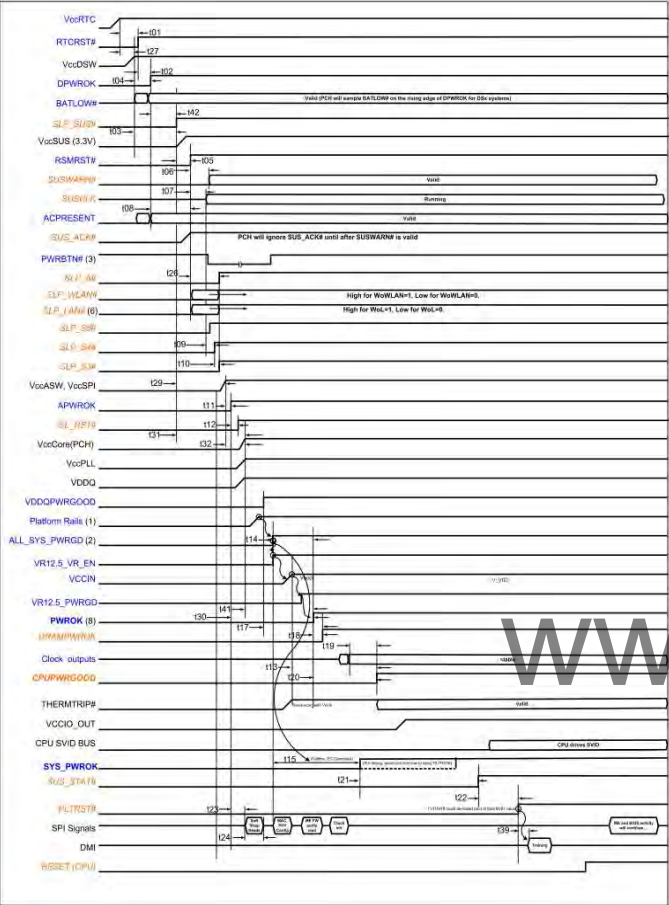
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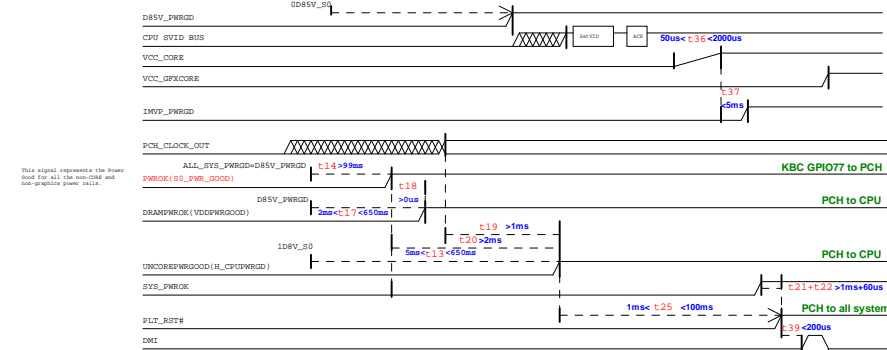
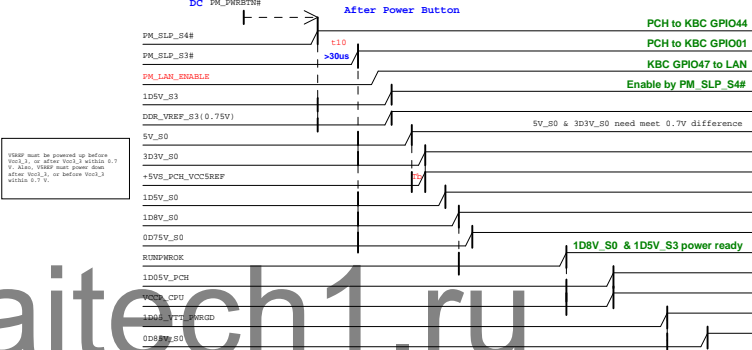
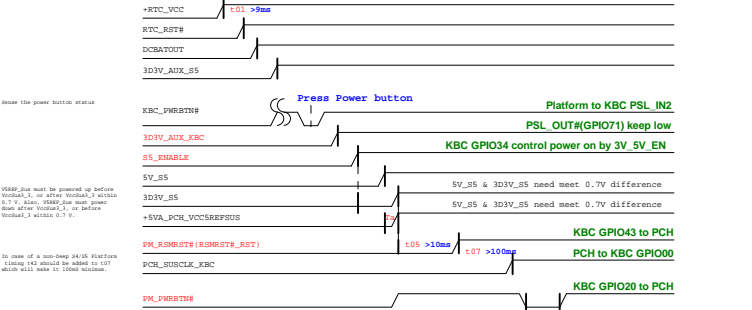
Date: Thursday, March 07, 2013

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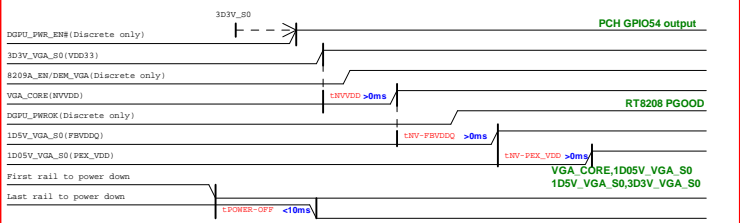
Shark Bay Platform Power Sequence



(DC mode)

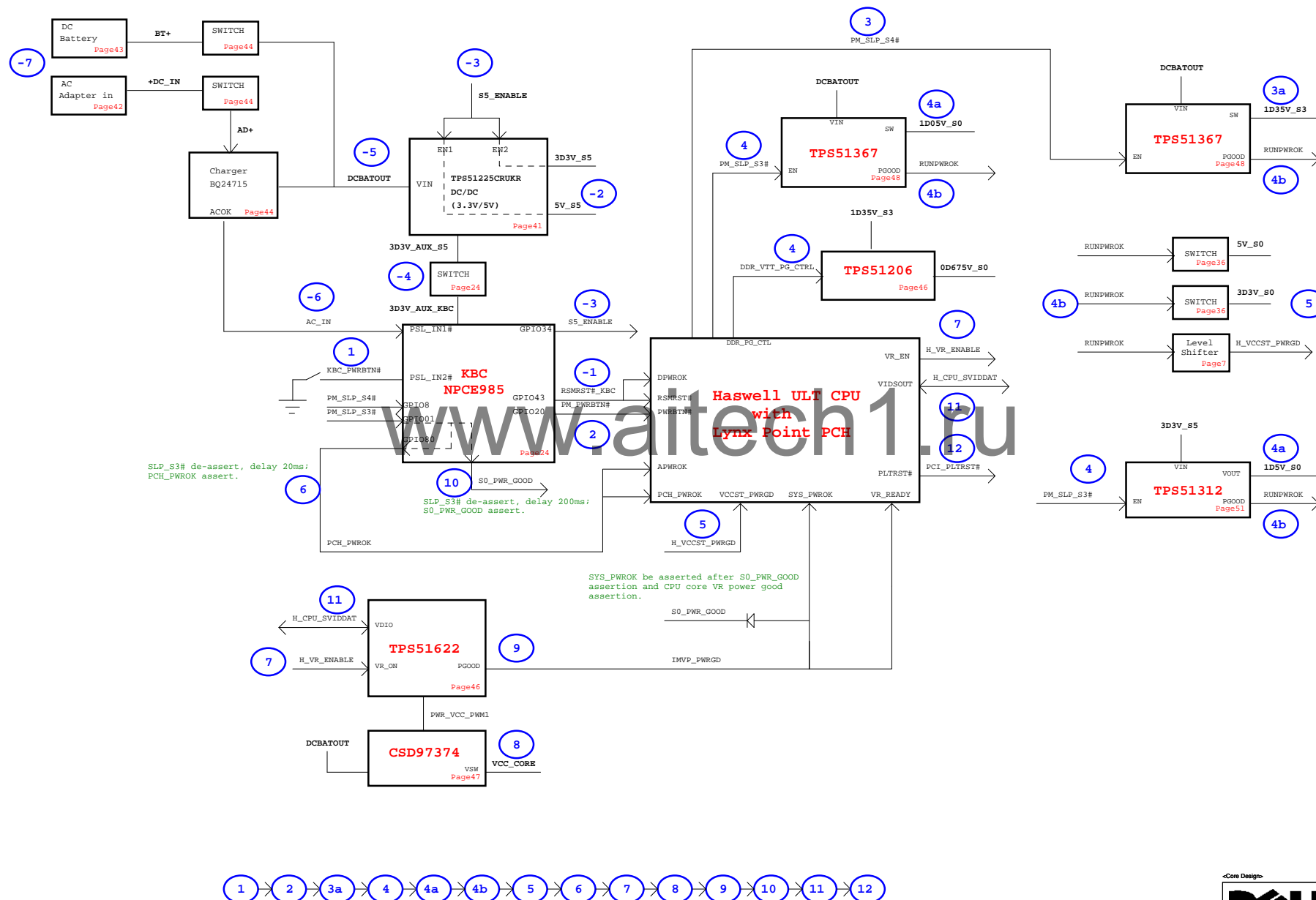


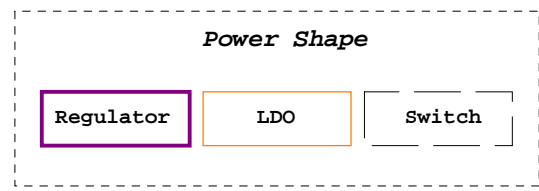
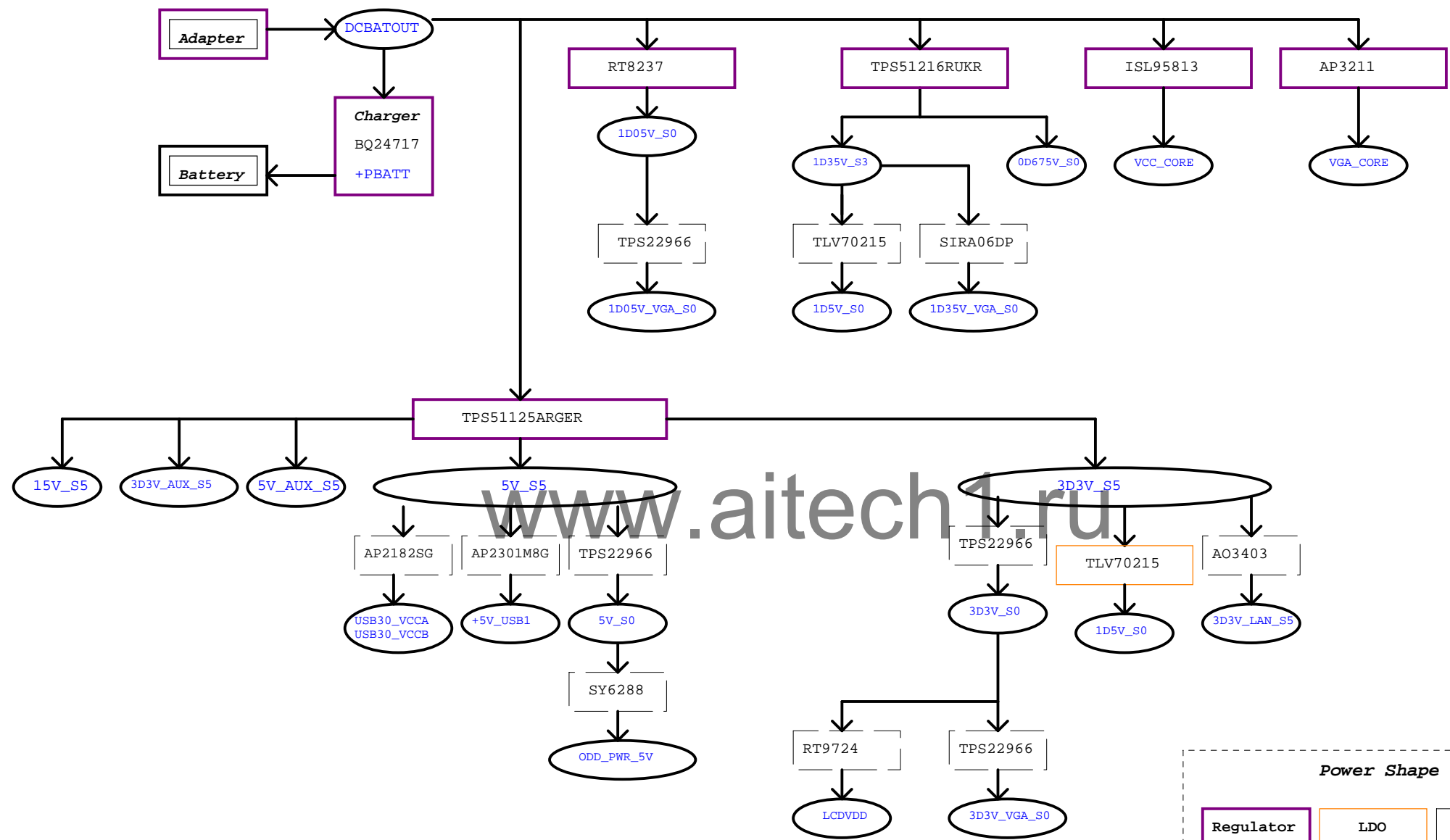
N14P-GT Power-Up/Down Sequence



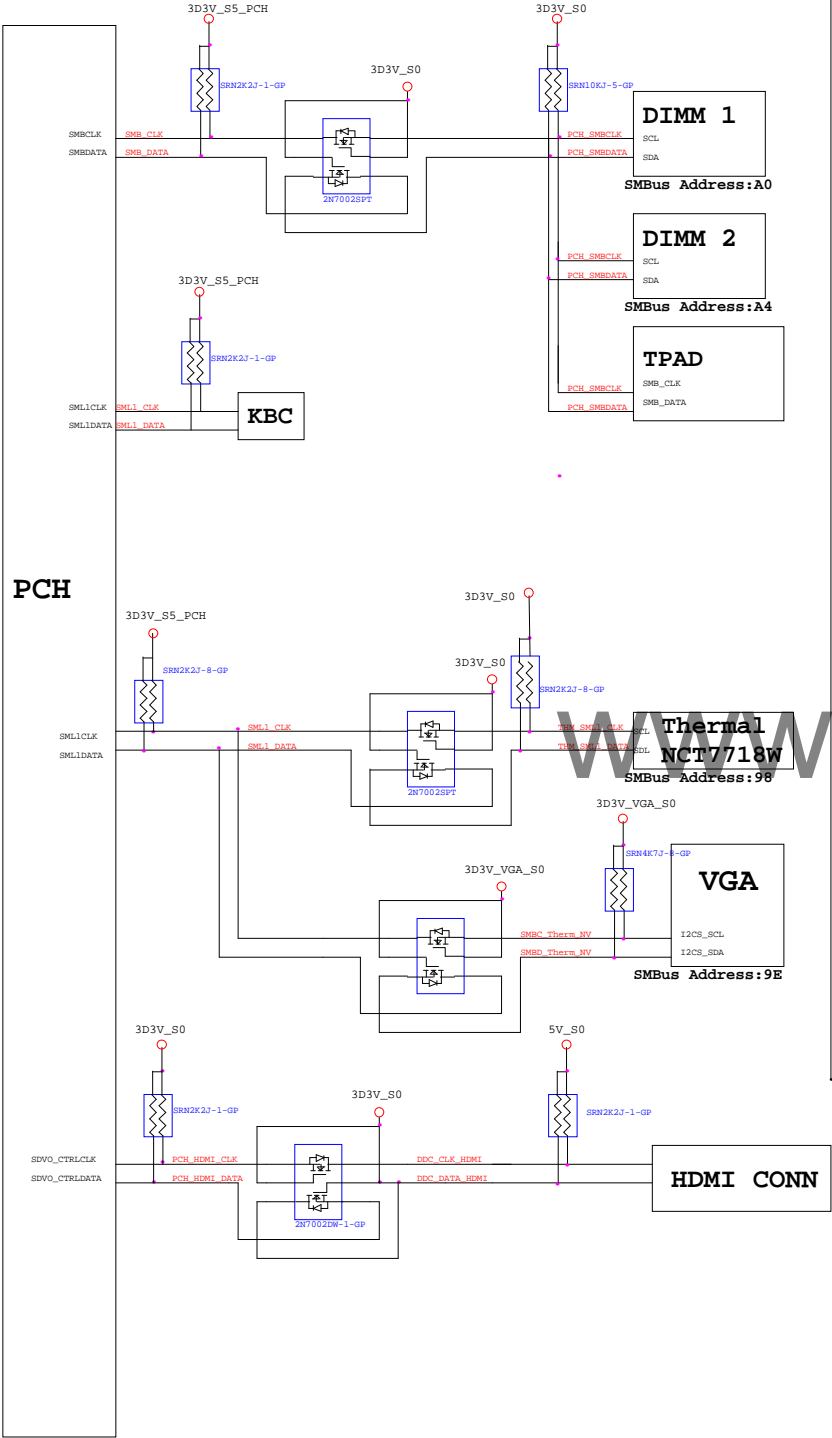
For power-down, reversing the ramp-up sequence is recommended.

# Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

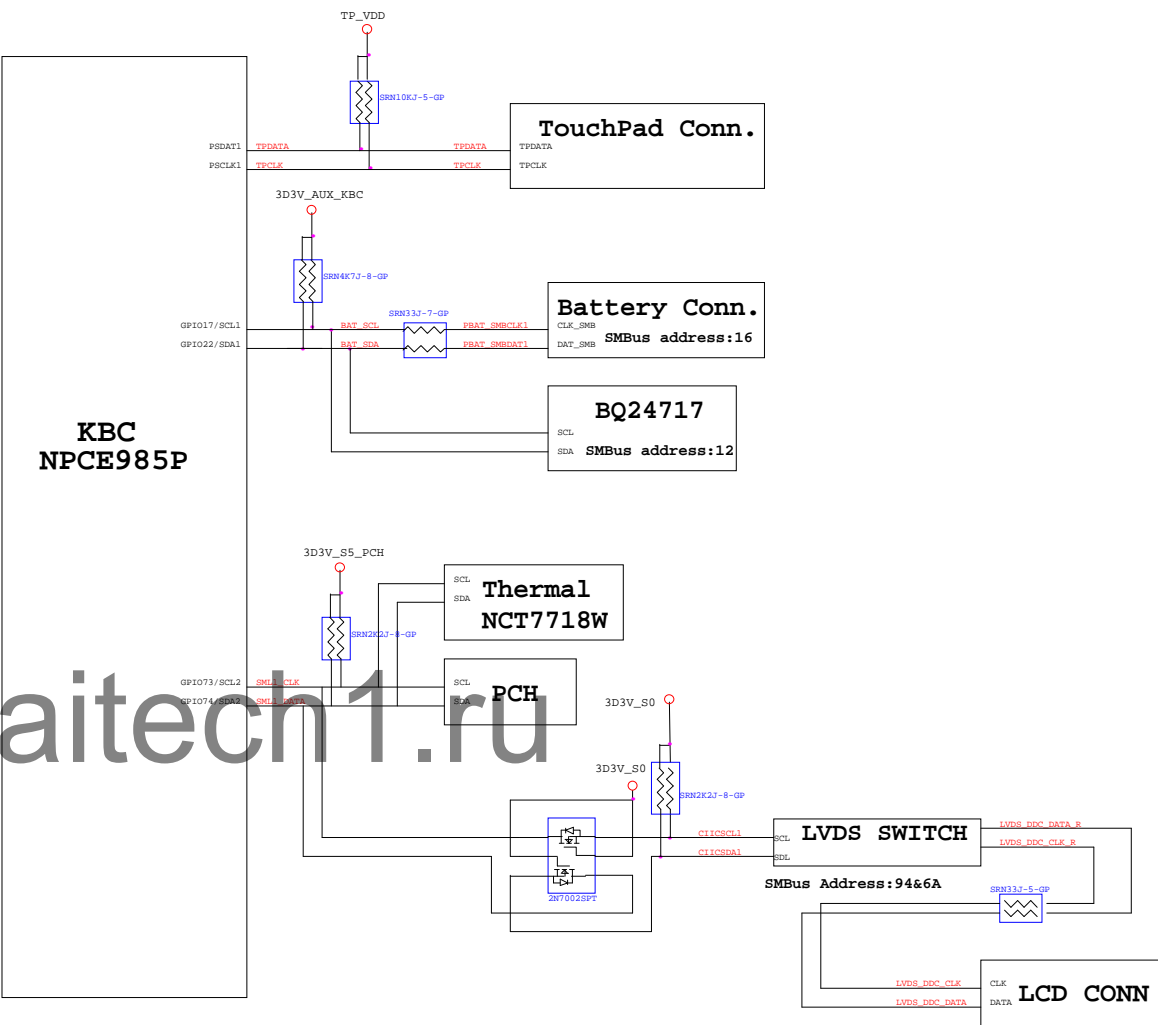




PCH SMBus Block Diagram

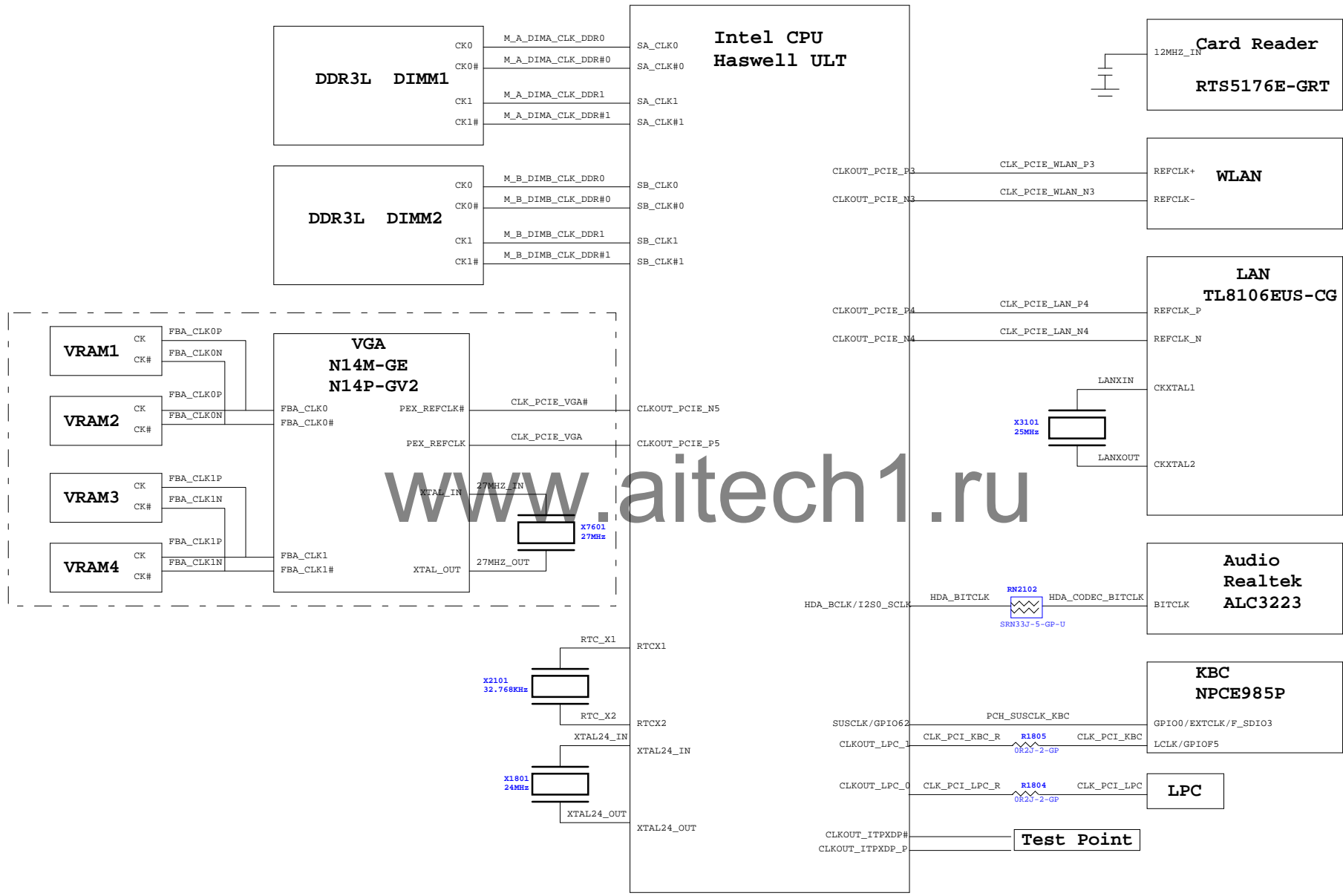


KBC SMBus Block Diagram

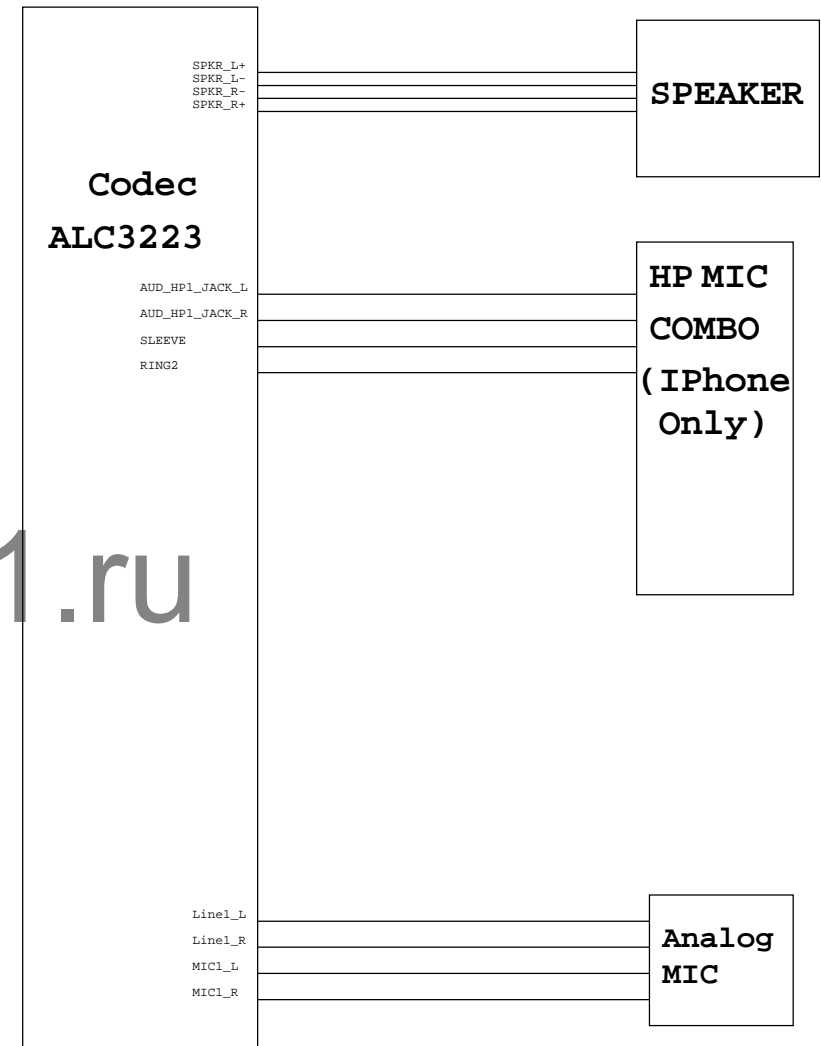




OAK Haswell CLK Block Diagram



### Audio Block Diagram






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